String Current Unbalance Protection and Faulted String Identification for Grounded-wye Fuseless Capacitor Banks

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Introduction

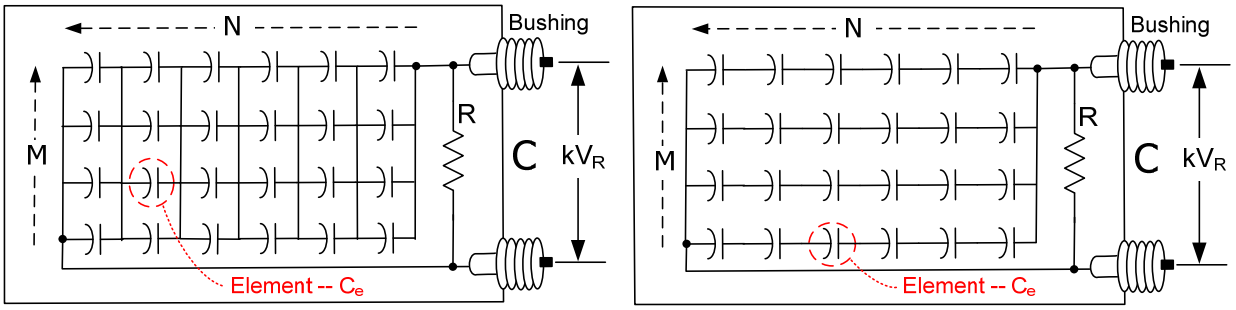
This paper discusses a new and unique concept of unbalance current protection and faulted string identification for three-phase shunt capacitor banks using fuseless capacitors. First, the relevant aspects of fuseless capacitor unit and shunt capacitor bank designs are discussed. Then basic unbalance current protection concepts that are commonly used are reviewed. Using known unbalance protection concepts an application to detect unbalanced current that may exist between the capacitor strings of the same phase and identify the phase and string in which the faulted units are located is discussed. Also, as a secondary measure the string currents of one string of each phase (i.e. phase A - string 1, phase B, string 1, phase C, string 1) are summed to detect unbalance between the phases. Current input and measurement to provide maximum sensitivity and ct application are also addressed. Further, using modern communication technologies, alternate protection and control configurations are suggested.

Shunt Capacitors

High voltage shunt capacitor banks are applied to high voltage electric power transmission systems in order to provide better system voltage regulation and more efficient power delivery across the transmission grid. Shunt capacitor banks are composed of different arrangements of capacitor units that are generally rated from 5 kV (kilovolts) to 25 kV with a kvar (kilovolt-amperes reactance) rating of 100 to 1000 kvar. The capacitor banks may be applied grounded or ungrounded. There are many shunt capacitor bank designs and methods of protection that are applied at all sub-transmission and transmission voltage levels up to 765 kV. The application and protection of shunt capacitor banks are discussed in References 2 and 3.

Fuseless capacitor Unit

Figure 1 shows two basic construction arranges of a fuseless capacitor units. The units are made up of a number of capacitor elements connected in parallel and series. A resistor, R, is connected across the capacitor unit terminals (bushings) to allow discharge of the voltage that is trapped on the capacitor unit when the capacitor bank is opened. Figure 1(a) shows a number of parallel capacitor element groups in series and Figure 1(b) shows a number of series element groups in parallel. In the units of Figure 1(a) each series element group contains a number of paralleled elements that are insulated foil capacitors. The capacitor elements are contained within a metal container and connected as shown to two voltage insulated bushings for external connections. The internal capacitor elements are insulated to designed voltage basic insulation [withstand] level (BIL) with a solid insulation film and insulating liquid. The failure mode of the capacitor unit is an insulation film failure across one of the element foil capacitors effectively shorting out the entire parallel element group. This causes the capacitance value of the capacitor unit to increase (capacitive reactance to decrease) and results in a voltage increase across the remainder of the series capacitor element groups and units in the string (Figure 2). A similar analysis can be made of Figure 1(b).



(a) Parallel connectec unit (b) Series connectec unit

Figure 1. Capacitor Unit, N is the number of series elements, M is number of parallel elements and $C = C_e(M/N)$ is the unit capacitance and kV_R is rated voltage

Rating

The following ratings are from IEEE Standard references 1, 2 and 3 and should be considered when applying and protecting capacitors.

The capacitance of a unit shall not vary more than -0% to +10% of the nominal value based on rated kvar, voltage and frequency, measured at 25°C uniform case and internal temperature. This range of capacitance allows for manufacturing tolerance. In reality this variance is rarely more than 6% or 7%. This variance must be considered when building capacitor banks and is an important consideration when considering unbalanced current or voltage protection.

Capacitors are intended to be operated at or below their rated voltage, but may be operated continuously up to 110% of their fundamental frequency voltage rating and at 120% of their rated peak voltage including all harmonics, but not transients. In addition exposure to momentary fundamental frequency overvoltage is permitted up to the values shown in Table 1. Such exposure is limited to 300 occurrences without loss of service life.

Table 1. Maximum permissible capacitor voltage

Duration (seconds)	Maximum Voltage (per unit of rated)
0.1	2.2
0.25	2.0
1.0	1.7
15	1.4
60	1.3

Since kvar is directly proportional to the unit's capacitance value C, the unit's kvar output at rated voltage and frequency will be 100% to 110% of its rated value depending on the actual value of C. [References 2 and 3 state the maximum kvar to be 115% for rated voltage and frequency. These references are based on an earlier version of reference 1]. In addition the unit must be designed to thermally provide additional kvar to support the overvoltages discussed above. Considering these factors the capacitor units are designed for continuous operation up to 135% of rated kvar. Similarly, the continuous current capability including all harmonics is 135% of rated current as well.

High Voltage Fuseless Transmission Capacitor Banks

Fuseless capacitor banks are designed with a large number of capacitor units of the same design connected in P parallel series strings of S units/string in each phase as shown in Figure 2.

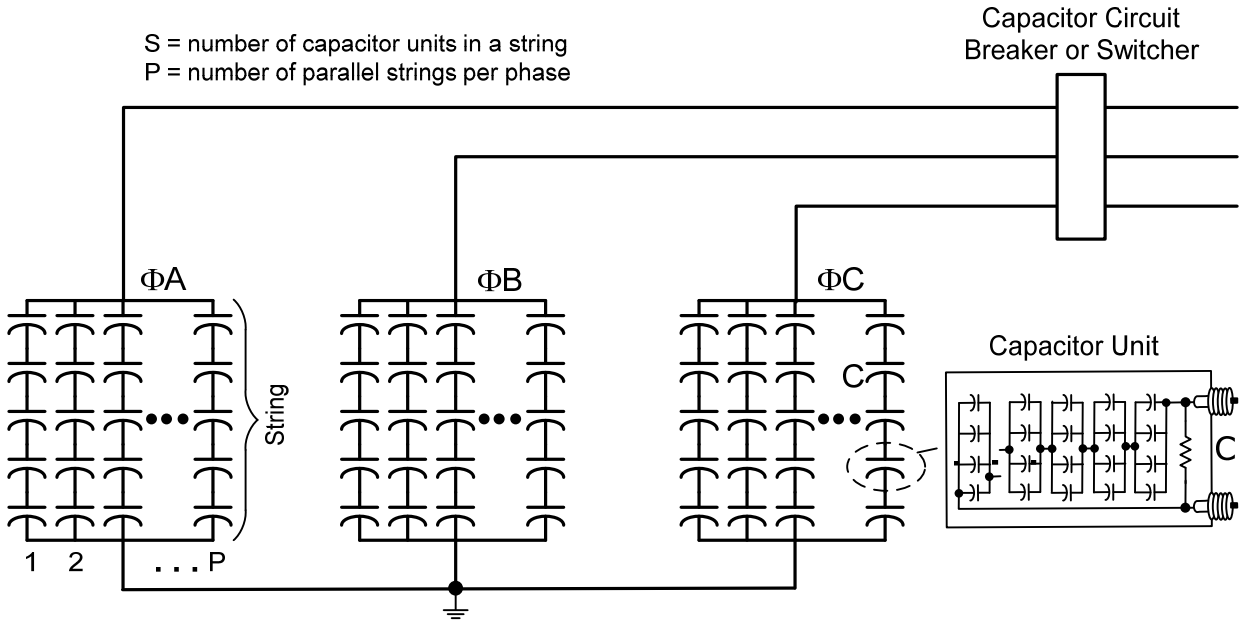


Figure 2. Typical High Voltage Three-phase Grounded-wye Fuseless Shunt Capacitor Bank

Table 2. Nameplate deviation markings for ABB ANSI fuseless capacitors

Deviation in %		Deviation Code
from	to	
0.000	0.499	0
0.500	1.499	+1
1.500	2.499	+2
2.500	3.499	+3
3.500	4.499	+4
4.500	5.499	+5
5.500	6.499	+6
6.500	7.499	+7
7.500	8.499	+8
8.500	9.499	+9
9.500	10.00	+10

Considering that capacitor banks can be made up of a very large number of capacitor units with different capacitance values due to manufacturing tolerance, it is readily obvious as to the potential impedance unbalance, and the resulting current unbalance, that may exist between the strings and phases of the bank. Manufacturers measure each unit's capacitance after manufacture and generally show the capacitance % deviation from rated on the unit's name plate per Table 2 or in other documentation. These markings are not covered in standards so check with the manufacturer.

Using the deviation codes capacitor units are arranged in the capacitor bank to equalize the string and total phase capacitance as much as possible. The process used generally results in the strings being balanced to within less than 0.5%. Therefore, you would normally not expect a variance of string current of more than 0.5% for normal operating conditions.

Unbalance Protection

The functions of unbalanced protection for fuseless shunt capacitor banks are to:

- Provide early unbalance alarm signals to indicate failures (shorting) of capacitor element groups within capacitor units and to trip for unbalances that are large enough to indicate that continued operation would result in further damage to the capacitor bank.
- Trip the bank for arcing faults that occur in the capacitor bank structure external to the capacitor units.

Capacitance and Measurement Unbalance

The primary unbalance that exists on all capacitor banks is due to basically two factors: system voltage unbalance and inherent capacitor bank unbalance due to manufacturing tolerances. Secondary unbalance errors may be introduced by sensing device tolerance and variation and by relative changes in capacitance due to the variance in capacitor unit temperatures throughout the bank. Efforts should be taken to minimize these unbalances.

System Voltage Unbalance

Unbalance current applications that are commonly used are shown in Figures 4. There are other commonly used unbalance current and voltage schemes, but they are not discussed here. Any scheme such as that of Figure 4(a) using a single neutral quantity, either voltage or current, to provide unbalance protection for the capacitor bank is subject to incorrect operation due to system voltage unbalance. During system ground faults there may be a substantial voltage unbalance measured by the unbalance relay and tripping will occur if appropriate means to block operation are not employed. Therefore, operation of the unbalance protection due to system unbalanced should be prevented with trip blocking logic or delayed tripping coordination with the system event.

Different capacitor bank arrangements, such as the split wye configurations shown in Figures 4(b) and 4(c) allow ct connections that cancel the effect of system voltage unbalance. Such configurations are generally applied at transmission voltage levels.

Manufacturing Tolerance

As previously discussed the manufactured unit capacitance can range from 100% to 110% of its calculated value using the unit's rated kvar, kV and frequency. Percent error markings are shown on each unit. Capacitor units can generally be strategically placed within the bank to cancel differences and minimize unbalance between strings and phases. Generally the unbalance between strings and phases can be reduced to less than 0.5%.

Capacitor Unit Temperature Effect

Unit capacitance varies with temperature and the variance of unit temperatures throughout the capacitor bank is very much dependent on the construction of the bank and environment. For example on a hot summer day some of the bank may be shaded while other parts of the bank are in the baking sun. Therefore, it is important to know and understand the variance and take it into account. Figure 3 shows the per unit capacitance (C_T / $C_{25°C}$) variance with temperature for capacitor units impregnated with Faradol 810, an insulation fluid used by ABB.

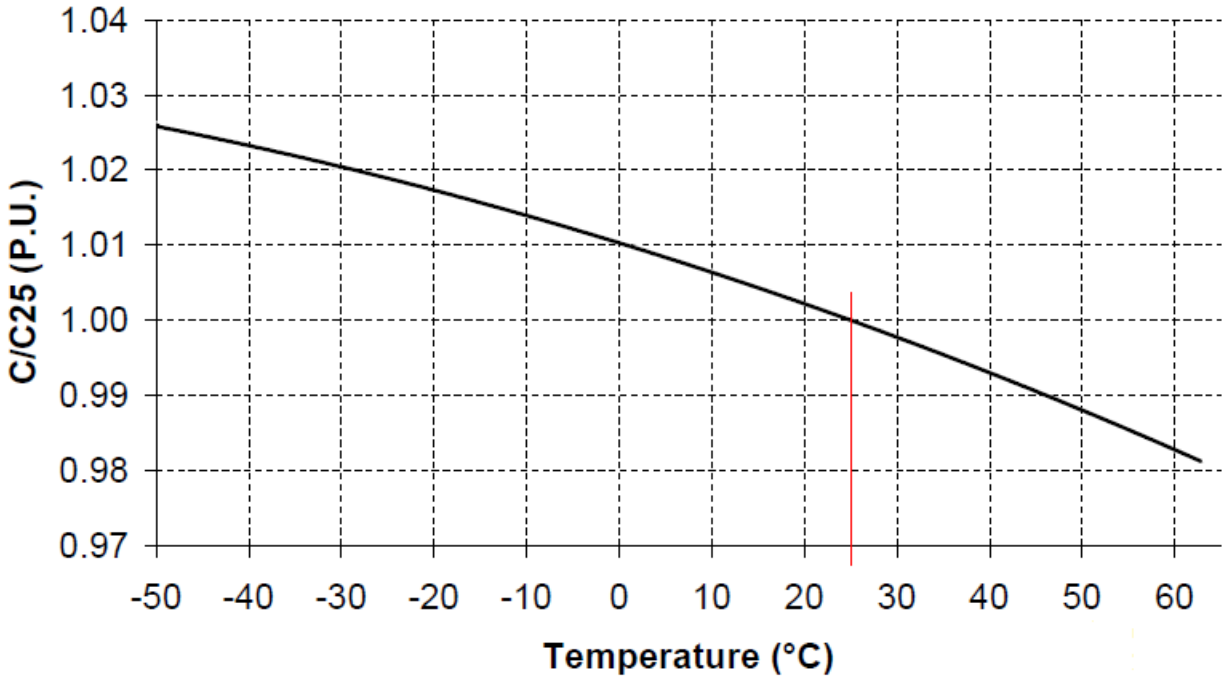


Figure 3. Per unit capacitance of the 25°C rating vs. temperature for capacitors impregnated with Faradol 810 insulating fluid

Sensor Variance

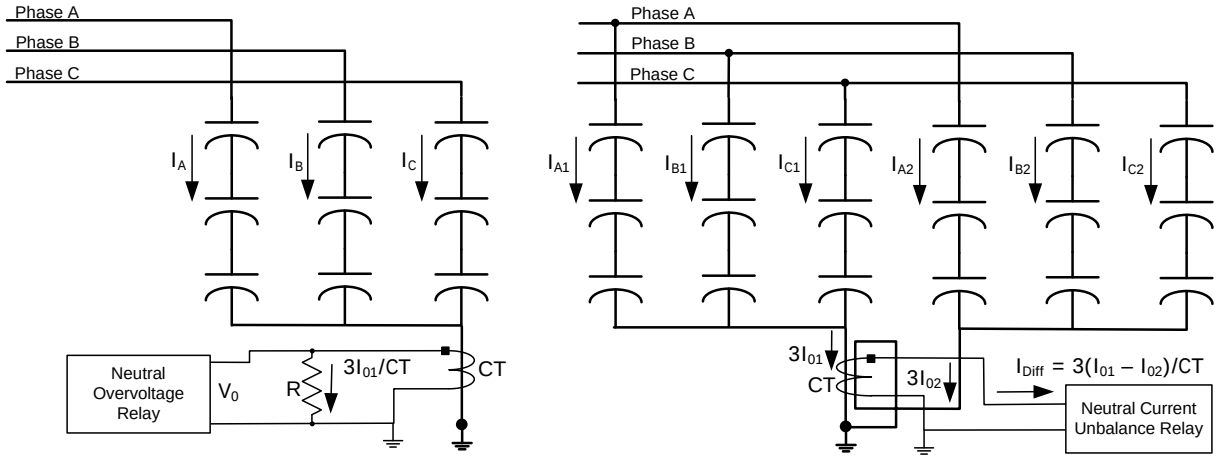
Current and voltage transformers should be selected to meet the application requirements. Generally this is of no concern as long as the secondary string current is less than rated secondary current and the ct accuracy and burden requirements are met. Careful attention should be given to the burden since the application may involve small cts with C10 burden ratings and long ct leads between the capacitor bank and control house. Also, identical current transformers (i.e. same manufacturer, rating, etc.) are recommended for unbalance current application requiring multiple current transformers to minimize measurement variances.

Current Unbalance Schemes

Neutral current unbalance

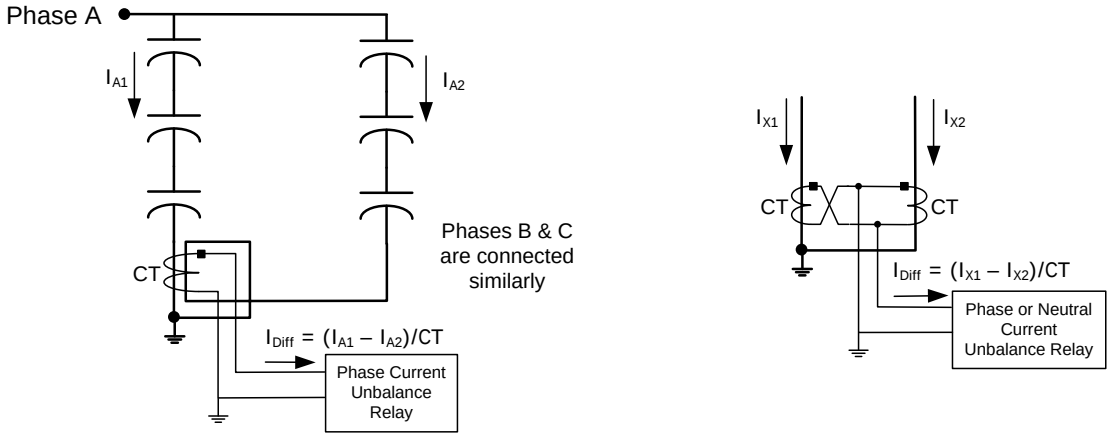
Figure 4(a) shows a neutral current unbalance protection scheme for a single wye-grounded capacitor bank. In this scheme a low ratio ct, a load resistor and an overvoltage relay are used to achieve required sensitivity. The relay measures a voltage proportional to the neutral current $3I_0$. This scheme is generally limited to lower MVAR banks. This scheme is shown to illustrate the impact of system unbalanced voltages on protection schemes. Tripping should be delayed in the event of system voltage unbalance due to system faults until the fault has cleared. If there are other anticipated voltage unbalances such as load that may cause operation of the unbalance relay then appropriate compensation of the unbalance should be made or another scheme should be used.

Figures 4(b) and 4(d) show two methods of connecting the neutral cts of a split wye-grounded capacitor bank. The split bank consists of two identical wye-grounded bank halves with their neutrals and neutral cts connected as shown to measure difference current between the two half bank neutrals. Using either of these neutral unbalance connections will eliminate the effect of system voltage unbalance since both bank halves respond to system voltage conditions identically. For these schemes only unbalance current due to inherent unbalance, failed elements and arcing faults is measured.



(a) Ct neutral connection for single bank into an overvoltage relay ($V_0=3RI_0$)

(b) Single ct neutral connection for split bank



(c) Single ct Connection between A phases of a split bank

(d) Alternate two ct connection of neutrals or common phases of a split bank

Figure 4. Unbalanced phase and neutral current protection of fuseless wye-grounded capacitor banks

Phase current unbalance

Figure 4(c) and 4(d) show two phase current unbalance protection schemes for a split wye-grounded banks where the individual phase currents of the bank halves are compared. Only phase A is shown. Using either of these phase unbalance schemes will also eliminate the effect of system voltage unbalance since the phases of both bank halves respond to the system phase voltage conditions almost identically. The only difference being the inherent unbalance between the phases of both halves. For these schemes only unbalance current due to inherent unbalances, failed elements, phase voltage rises above rating and arcing faults is measured.

Fault Voltage Rise

Phase-to-ground overvoltage will occur to some degree on the non-faulted phases during a single phase-to-ground fault on grounded systems. For effectively grounded systems, which are defined by the ratios of equivalent system parameters $X_0/X_1 \leq 3.0$ and $R_0/X_1 \leq 1.0$ [5], the maximum phase-to-ground voltage on the non-faulted phases during a phase-to-ground fault is about132%. There is likewise a 132% increase in the string current and in any unbalance current being measured.

For phase current unbalance measurement, voltage rise is only an issue when there is a substantial unbalance due to pre-existing capacitor element failures at the time of the fault. The pre-existing unbalance would have to be in the order of 70% of the relay's trip setting to effect a trip for a healthy

phase fault voltage rise to 130% of rated. Since there are significant failed elements, it may be that tripping is acceptable. However, for continued availability of the capacitor bank after the system fault tripping should be delayed.

Ct ratio compensation

Figure 5 shows the ct connections to a simple numerical relay scheme to provide unbalance current protection with ct ratio compensation for inherent unbalance. Factors k_1 and k_2, for example, can represent the respective ct ratio such that when multiplied by the measured secondary current yields the respective primary current. Normally k_1 and k_2 equal and I_{Diff} is zero when I_{A1} and I_{A2} are equal. If there is an inherent unbalance in the string or phase capacitance then I_{A1} and I_{A2} will not equal and I_{Diff} is not zero. For this case factors k_1 and/or k_2 may be adjusted to set I_{Diff} to zero.

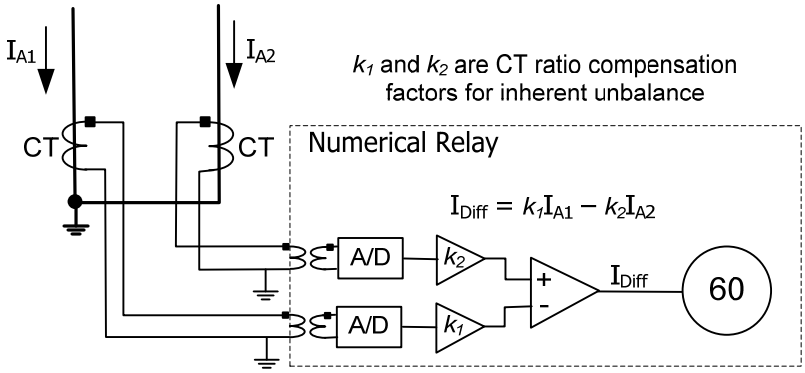


Figure 5. Unbalanced current protection with ct ratio compensation

Ambiguous Indication

Ambiguous indication occurs, for example, on the split banks of Figures 4 and 5 when an equal, or close to equal, number of failed elements exist on the same phase of the two bank halves. In this case unbalance current cannot be measured and voltages on the remaining units of the two parallel phases may exceed their capability. To address ambiguous indications it is desirable to set an unbalanced current alarm to indicate as few failed capacitor elements as possible. If an alarm occurs as a result of failed elements in one bank half and no corrective action is taken and then the alarm disappears, it indicates that failed elements now also exist in the corresponding phase of the other bank half and the failures are now masked. This sets up a potentially catastrophic condition.

Arcing Faults

Arcing faults occur in the capacitor banks, but external to the capacitor units. Arcing faults are the result of damaged or contaminated insulators or capacitor unit bushings. Since the faults are external to the capacitor units at least one or more can's worth of elements will be shorted and detected by current unbalance protection. Clearing of arcing faults with current unbalance protection must be secure, but should be fast enough to minimize damage to capacitor units. Trip delay times of 50 to 100 ms have been used for arcing faults.

Faulted string and unit identification

Any of the aforementioned unbalance current protection schemes only identifies that element failures exist somewhere in the capacitor bank. At best, phase current unbalance phase current schemes identify the phase. Element failures within the fuseless capacitor unit are not visible and therefore considerable time must be spent locating and replacing failed units.

String Current Unbalance

The previous discussion discussed unbalanced neutral and phase current measurement using two cts measuring normally equal currents and taking their difference to determine any unbalance for abnormal conditions. This same principle can be applied on a broader scale to provide individual string unbalance monitoring and more reliable current unbalance protection. String current measurement of all the individual strings on all phases of the capacitor bank provides the possibility of both unbalance current protection as well as faulted string indication. This protection is economically provided based on using a low voltage (600 V, 10 kV BIL) window type ct [as opposed to wound type cts] at the grounded end of each capacitor bank string. The window type ct has a very low susceptibility to voltage transients. The applied current transformers' ratio and accuracy (burden) class should be selected to assure accurate secondary current measurement and sensitivity as is done with existing methods of phase and neutral current unbalance protection. The ct application is discussed in more detail in a later section.

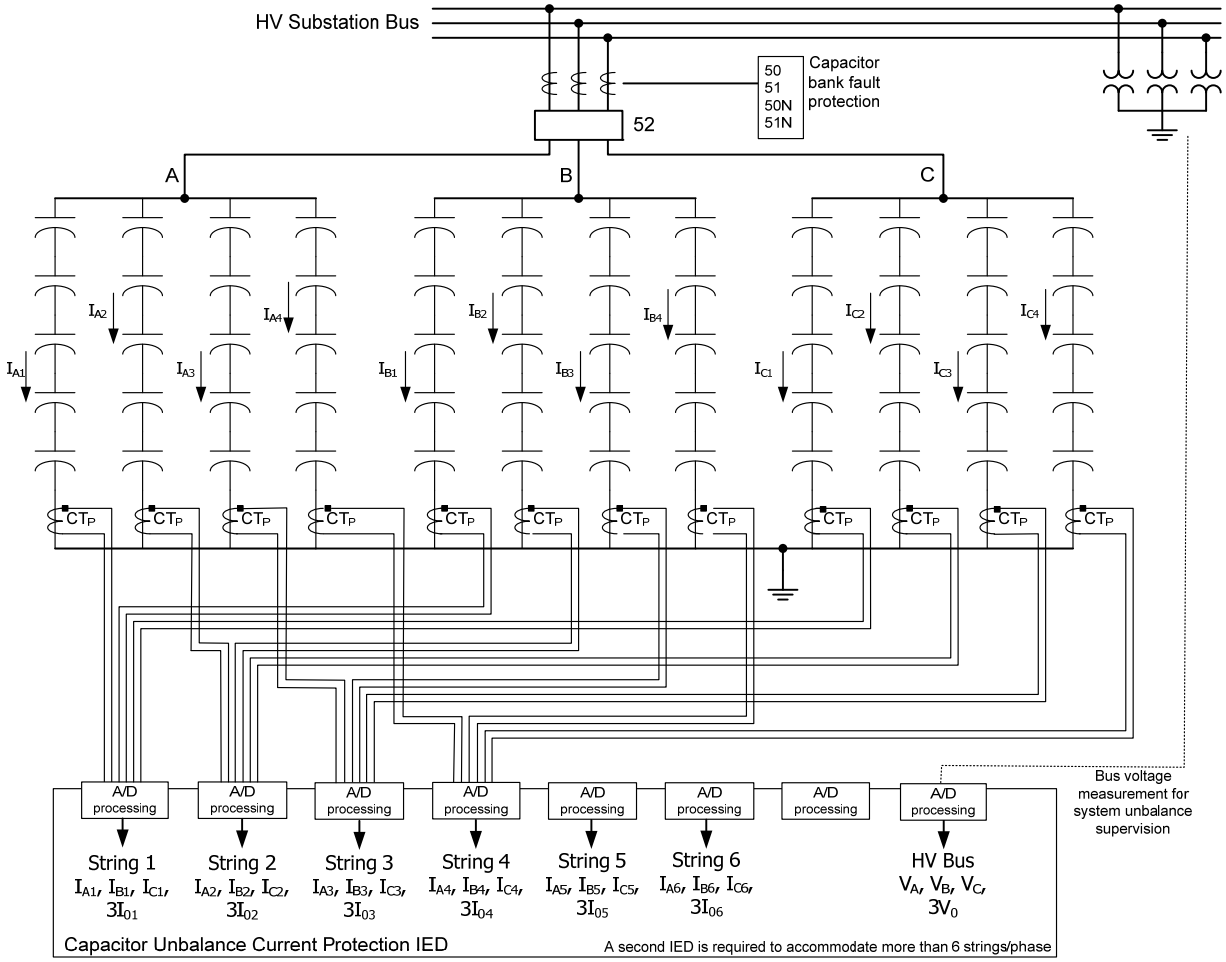


Figure 6. Basic three-phase ct and unbalance current protection IED and ct connections to a bank with 4 strings per phase.

Figure 6 shows the basic three-phase capacitor bank configuration and ct connections to the unbalanced current protection IED (Intelligent Electronic Device). Each three-phase A/D (analog to digital) processor to which the cts and vts are connected provides the numerical (digitized) data of the analog signals input into that processor. Therefore, the common string (i.e. string 1, string 2, etc.) data of all three phases and ground ($3I_0$) can easily be provided to the application.

Two methods of string unbalance detection are discussed. The first and primary method is the continuous intra-phase current unbalance, which compares the string currents of adjacent strings within each phase (i.e. I_{A1} - I_{A2}, I_{A2} - I_{A3}, I_{A3} - I_{A4}, . . . , $I_{A(P-1)}$ - I_{AP}, I_{AP} - I_{A1}, P = number of strings/phase) and the second and complementary method is the common string residual, which measures the sum ($3I_0$) of the common string of each phase (i.e. $I_{A1} + I_{B1} + I_{C1}$, $I_{A2} + I_{B2} + I_{C2}$, . . . , $I_{AP} + I_{BP} + I_{CP}$).

Continuous intra-phase string current unbalance protection

The following discussion is based on phase A ct connections and the logic shown in Figure 7. Phases B and C are respectively duplicated. Each phase A string current $I_{A1,}$ I_{A2}, …, I_{AP} (P = number of strings/phase) is compared twice in a continuous loop around the phase (i.e. $\mathbf{I_{A1}}$ - I_{A2}, I_{A2} - I_{A3}, I_{A3} - I_{A4}, . . , $I_{A(P-1)}$ - I_{AP}, I_{AP} - $\mathbf{I_{A1}}$). This assures unbalance detection even in the most serious cases of ambiguous indication. Every string in the phase would have to have an equal number of failed (shorted) capacitor element groups for unbalance detection not to occur.

The primary string currents (1) I_{AJ}, (J = 1, 2, 3… P) are transformed to the secondary current value by the (2) current transformer CT_P where it is processed by the IED. Each string current is processed by the (3) A/D converter and the output numerical value may be adjusted by (4) k_{XJ} (X = A, B, or C for phase, J = string number). This allows adjusting the individual string ct ratios at commissioning to yield a common base current value such that all the digital string current values are very nearly equal (i.e. $I_{A1} = I_{A2} = I_{A3} = \ldots = I_{B1} = \ldots = I_{B4}$). This eliminates any unbalance due to manufacturing tolerance.

The differences in the compared string current values are taken (5) and then input into the appropriate unbalance current measurement function, 60S (6). The 60S measures the unbalance (difference) current and will alarm and/or trip at set threshold values of the unbalance current and time delay indicating failed capacitor elements in one of the two compared strings. The alarm settings, depending on the number series capacitor elements in the strings, are set at 25%, 50% and 75%, of the trip setting [or close them] to indicate strings with shorted elements while the capacitor bank is still operational. The faulted string can be identified by requiring an alarm level operation of both 60S-A functions that are in common with that string. This is done with logical AND gates (7). If, however, only one 60S-A function operates (8) there is an ambiguous indication meaning that there are a near equal number of failed elements in the two strings of the 60S function that did not operate. For example, if only Alarm 34 operates then either strings 2 and 3 or 4 and 1 have an equal number of failed elements. Tripping is done directly from the 60S-T unbalance detection function to assure fast and dependable tripping (9) when continued operation may result in further damage to the capacitor bank. This is particularly true if two adjacent strings happen to have an ambiguous indication (equal number of failed elements in two compared strings) such that unbalance cannot be measured and alarmed. In this case the second string comparison will operate. An ambiguous indication is unlikely, but possible. Making two unbalance current measurements with each string current and its two adjacent strings makes not tripping due to ambiguous indication considerably more unlikely. Further, there will always be an alarm or trip unless there are an equal number of failed elements in every string of the phase.

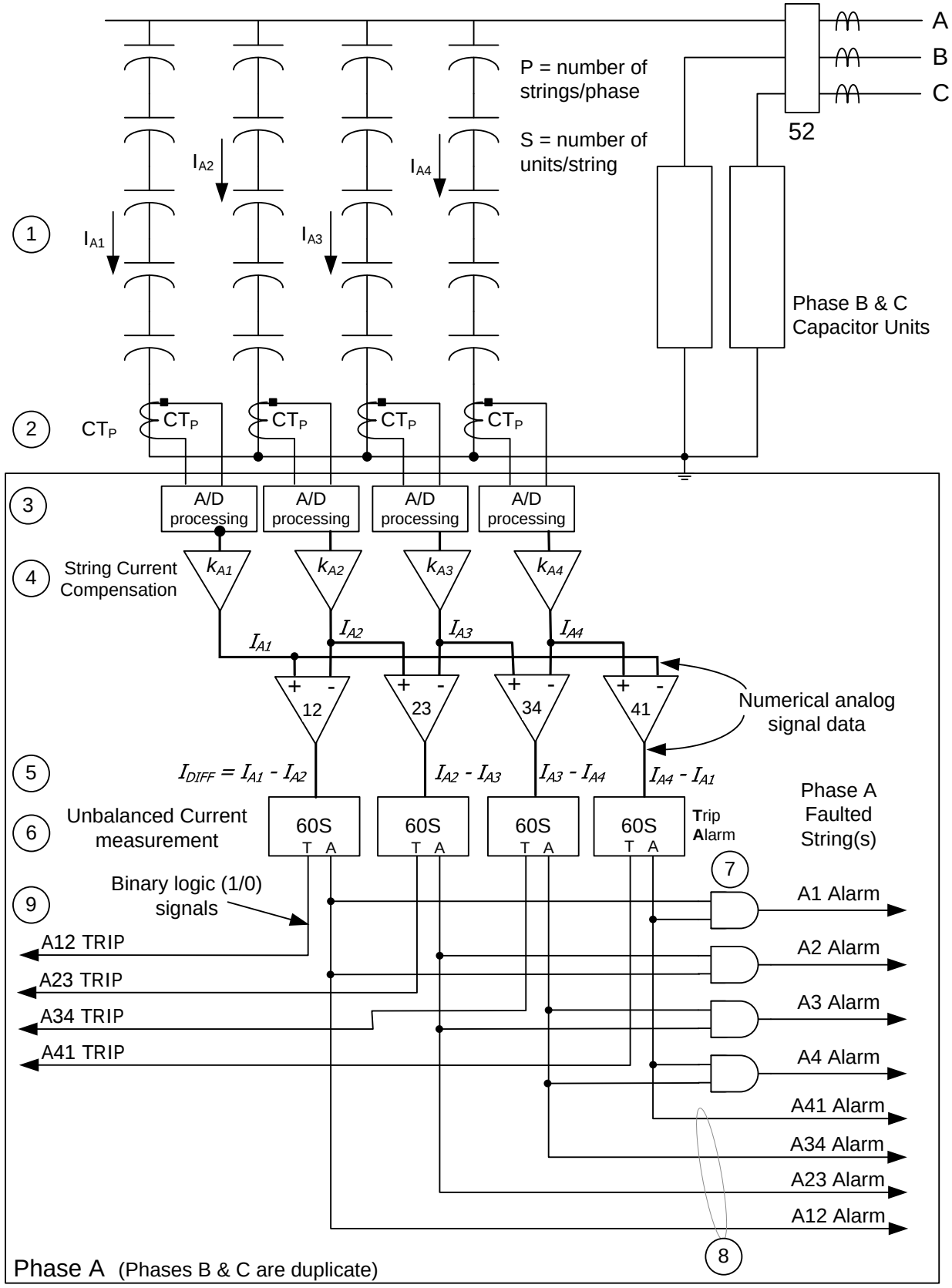


Figure 7. Continuous Intra-phase current unbalance - comparing adjacent strings of a four string per phase bank

Common String [Zero Sequence] Current Unbalance

The failed element detection and correct faulted string identification can be enhanced with the additional use of zero sequence current (3I0) measurement by summing currents of one string of each phase (i.e. phase A - string 1, phase B, string 1, phase C, string 1) to detect unbalance between them. The operation and logic is shown in Figure 8. There is no need for zero sequence current compensation (1) if the phase ct inputs have been correctly compensated. The 60N functions (2) will provide unbalance detection between corresponding strings on each phase. This detection method allows identification of the faulted string number and will assist in identifying the correct faulted strings in the case of ambiguous phase indications.

Zero sequence current in all strings of the capacitor bank will occur simultaneously for substation bus and system voltage unbalances. Preventing operation of the zero sequence current unbalance functions during these events is necessary. This can be done by two methods. The first is unbalanced bus voltage detection with a ground ($3V_0$) overvoltage function (59N) that is provided (3) to block operation of the 60N current unbalance functions during system unbalances. The second method of blocking the 60N trip function is by simultaneously measuring zero sequence unbalance currents in all strings (4). The latter method allows "current only" operation with no need for a voltage transformer.

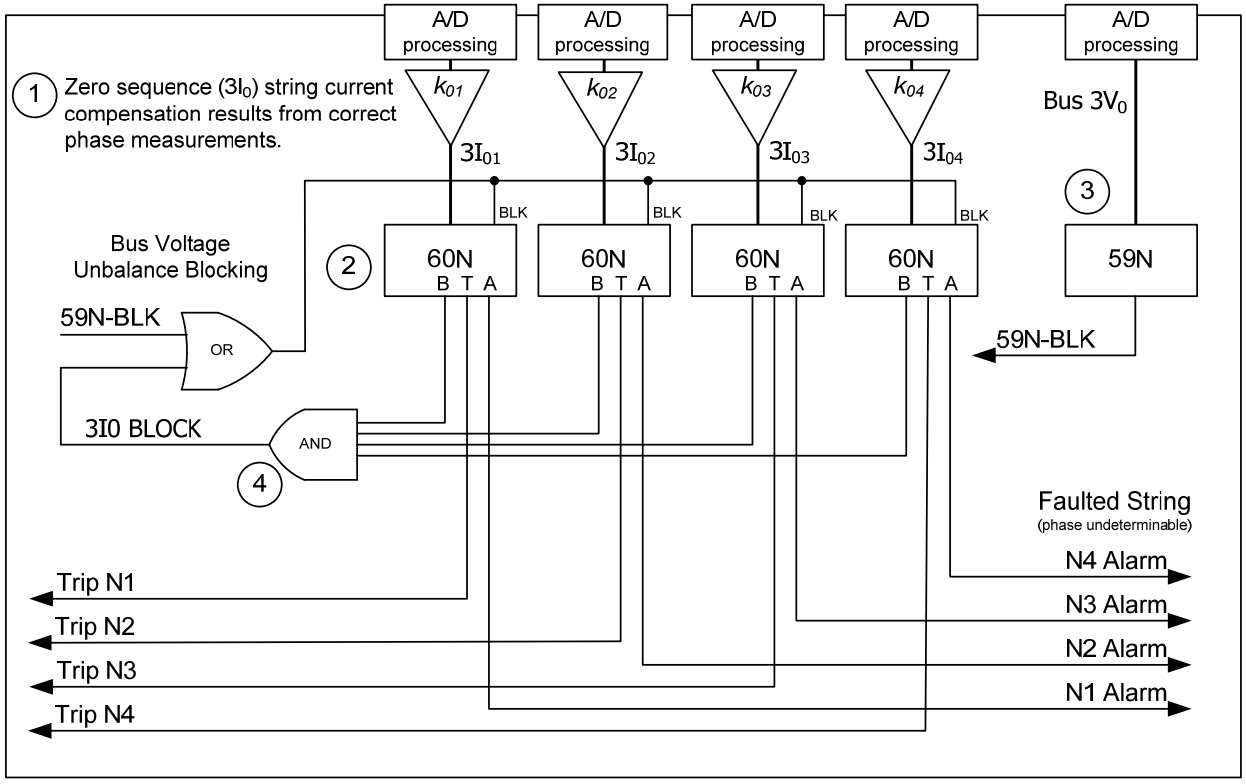


Figure 8. Residual ground current measurement - comparing corresponding strings on each phase.

The 60S and 60N Current Unbalance Functions

Each 60S and 60N current unbalance function is made of two different measurement functions for alarm and trip.

Alarm, 60S-A and 60N-A

The alarm units are very sensitive current monitoring functions each with 5 settable output levels. Each unit measures fundamental frequency current and operates with a 100 ms computation interval time to provide 0.5% measurement accuracy. Four of the settable outputs are used to provide unbalance current alarming at typically 2.5%, 5.0%, 7.5% and 10.0% of rated string current. Each alarm level has an alarm timer and will operate an LED, an output contact and a data point available for station HMI or SCADA monitoring using DNP-3 or IEC61850. Outputs may follow the alarm signal or latch. Timer settings are recommended from 2 to 60 seconds for latching alarms.

The 10% alarm level may also be used for tripping. Since the 10% alarm level is intended for monitoring capacitor element failures and not intended to address arcing faults, a trip time delay of 1.0 to 2.0 or more seconds is recommended.

Trip, 60S-T and 60N-T

The trip units are independent phase and ground overcurrent functions to provide fast tripping for unbalances greater than 10% of rated string current. Each unit measures fundamental frequency current and operates with an 8 ms computation interval time and provides 1.0 % measurement accuracy. The tripping units are particularly useful for detecting and removing arcing faults. They are typically set from 0.05 to 0.10 seconds for fast clearing of arcing faults. There are four settable overcurrent trip steps per 60S-T and 60N-T. This allows detection and tripping for rapidly escalating faults with higher unbalance current settings and shorter tripping time delays.

Ct Application

Low voltage (600 V, 10 kV BIL) window type cts have been used successfully for years in high voltage grounded capacitor bank applications. The window type ct is applied at the grounded end of each capacitor bank string as shown in Figure 9. It has no primary winding integral to its design. The primary is the conductor that passes through the ct window as shown in Figure 10. It has a very low susceptibility to voltage transients as opposed to wound type ct, also shown in Figure 10, which has a primary winding integral to its design and requires primary surge protection in capacitor bank applications. Regardless of the low transient voltage susceptibility of the window type ct, a 1000 V varistor (or comparable surge suppressor) is suggested for secondary winding and lead protection. The leads should be twisted pair routed in a grounded conduit back to the control house and grounded there. The non-polarity end if the secondary lead is single point grounded at the protection panel.

The ct ratio is selected to have 1 to 3 A secondary current and therefore a metering class ct is recommended to assure maximum accuracy. Better unbalance sensitivity is achieved with larger secondary current suggesting the use of a lower ct ratio, but this may result in limiting the ct burden capability. The maximum burden should limit the selected ct secondary voltage to operate well into the linear region of the ct's excitation characteristics below the ct rating.

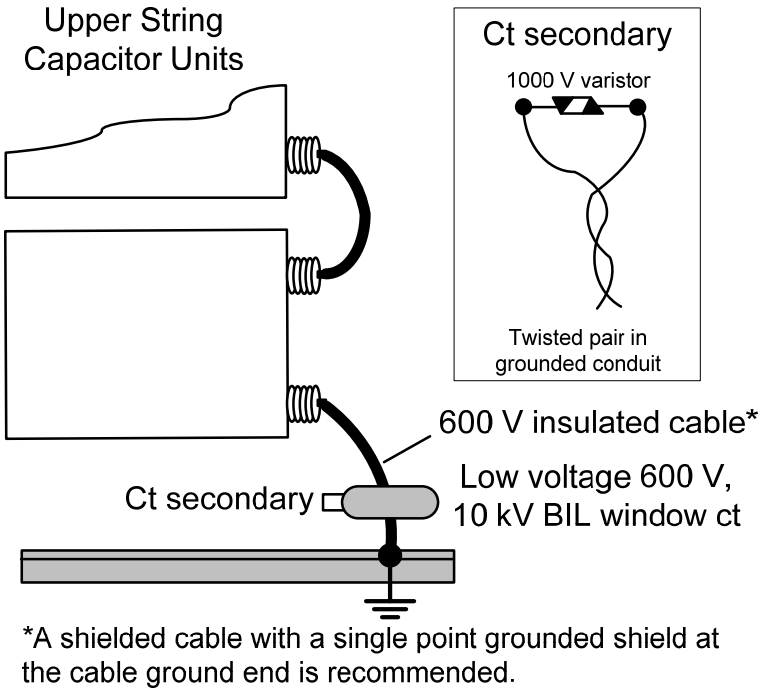


Figure 9. Low voltage ct application at the grounded neutral end of the string

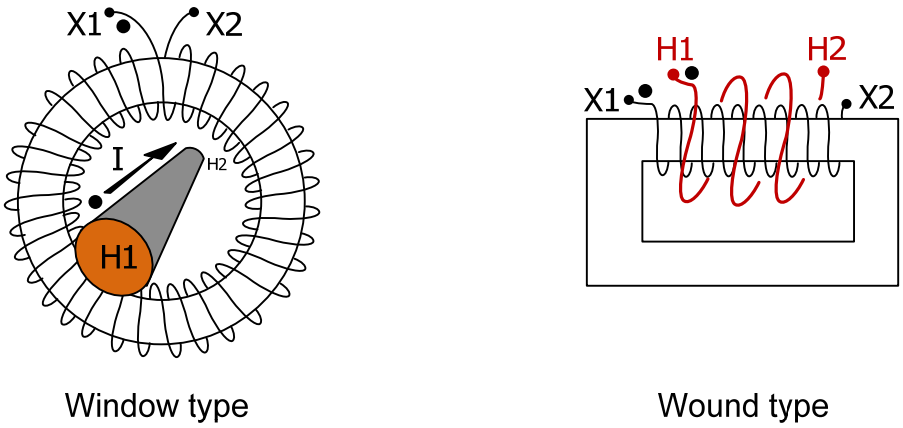


Figure 10. Window and Wound type current transformers

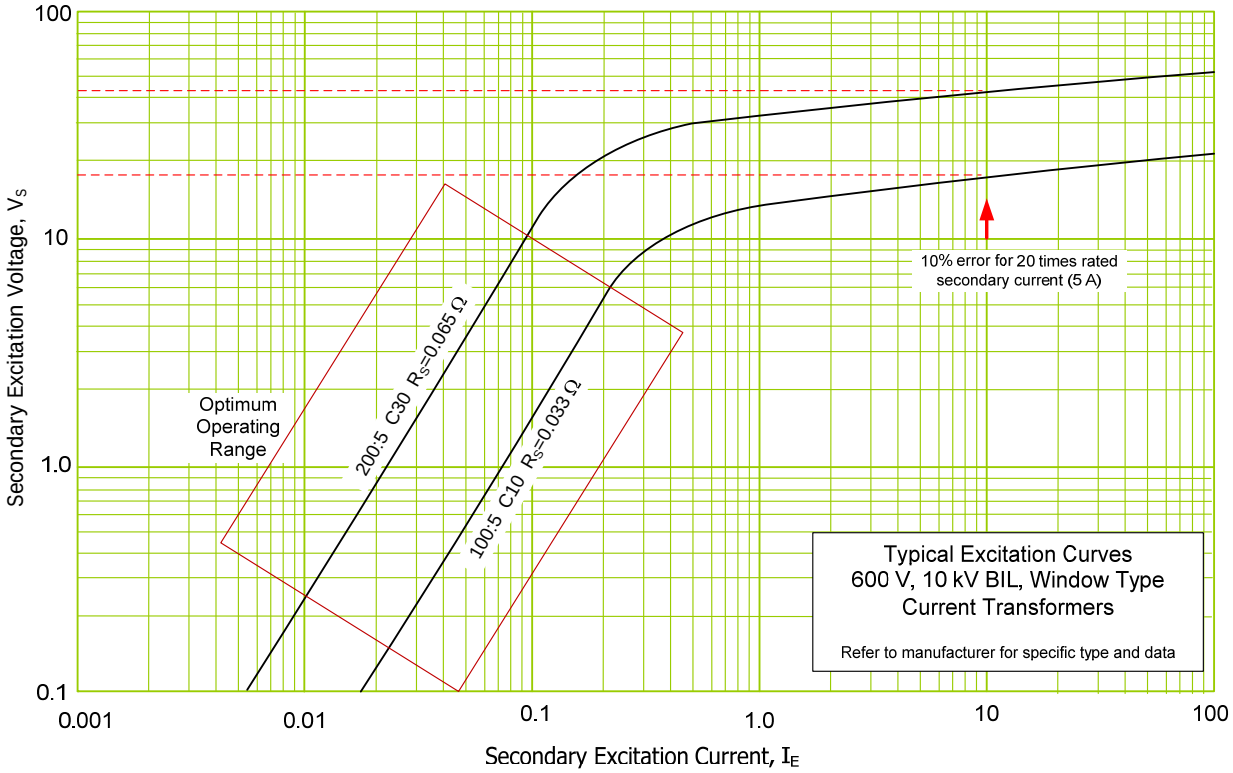


Figure 10. Typical window type 100/5 and 200/5 ct excitation characteristics

Analog Inputs

To achieve greater accuracy for string current measurement the string current analog input transducers are rated for 1.0 A. This provides a measurement accuracy of 0.01 A (1% of input rating) or better. These current inputs are normally connected to cts that have a rated secondary of 1.0 A, however, in this application the 1.0 A current inputs are connected to cts that have a 5.0 A rated secondary. The inputs can carry 4.0 A continuously. This is appropriate as the typical string current is 30 A to 60 A on the primary and 1.5 to 3 A on the secondary for a 100/5 ct. This also assures operation of the 100/5 in the more accurate region of its excitation characteristics with a reasonable burden.

Phase and String Identification

Trip and alarm logic is provided from the 60S and 60N trip and alarm functions. The appropriate logic for identifying the involved and string for an alarm or trip is shown in Figure 12. When there are no ambiguous indications the phase and string identification is straight forward. For example from Figure 7 A2 Alarm means there are capacitor element failures on phase A, string 2. If ambiguous indications exist one would not expect an equal number of failures in every string of a phase and much less in all phases. Rather, element failures would be expected in random string locations throughout the capacitor bank. Therefore, for alarm level element failures that result in these ambiguous indications logic is provided to identify the phase and string element failures accurately. For example if strings 2 and 3 have a number of element failures both above the alarm level and there were no other string element failures within the bank then phase A ambiguous indication alarms A12 Alarm and A34 Alarm would occur as well as the neutral unbalance alarms N2 Alarm and N3 Alarm. With these alarm operations phase A strings 2 and 3 can be readily identified using the logic of Figure 12 and the resulting information of Table 3. Using this simple logic there is no realistic scenario where the phase and string with an alarm level of failed capacitor elements cannot be identified.

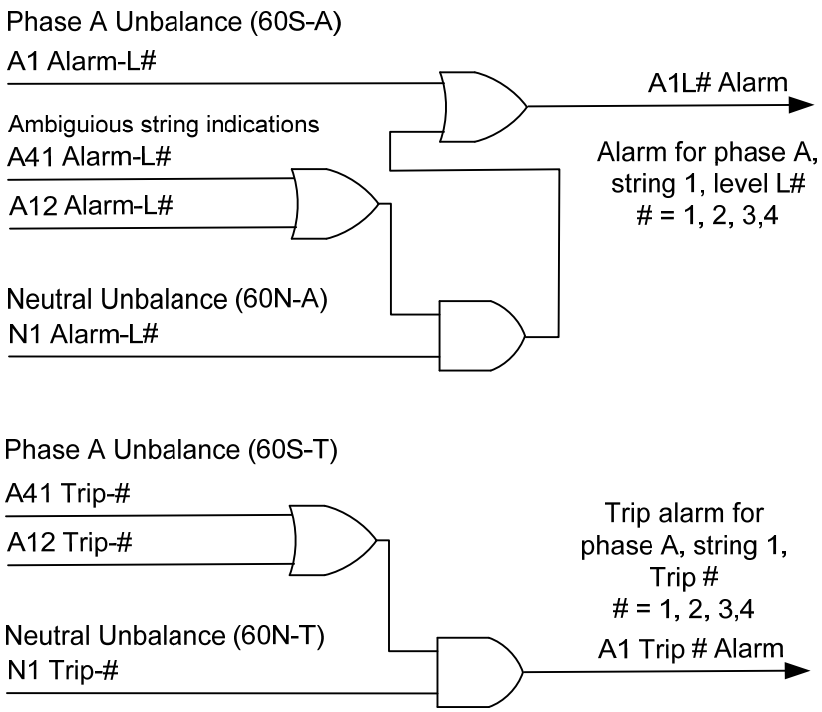


Figure 12. Unbalance level and trip alarms for phase and string identification

Table 3. Phase A string identification with ambiguous indications

Phase Alarms	Neutral Alarms	Affected Strings
A41 Alarm A12 Alarm	N1 Alarm	1
A12 Alarm A23 Alarm	N2 Alarm	2
A23 Alarm A34 Alarm	N3 Alarm	3
A34 Alarm A41 Alarm	N4 Alarm	4

Event Reports

Up to 96 binary point statuses may be included in both the SOE (sequence of events) and DFR (digital fault record). The SOE showing the most recent 1000 operations is available for viewing from the front panel HMI or with interconnected computer software. An SOE event is added to the SOE list with a change of state of a binary point. The DFR records up to 40 analog signals in addition to the binary point status. The DFR can be set to trigger an event record on the operation of any alarm or trip operation. Also, pre-fault and post fault times are settable to record up to a 10 second record.

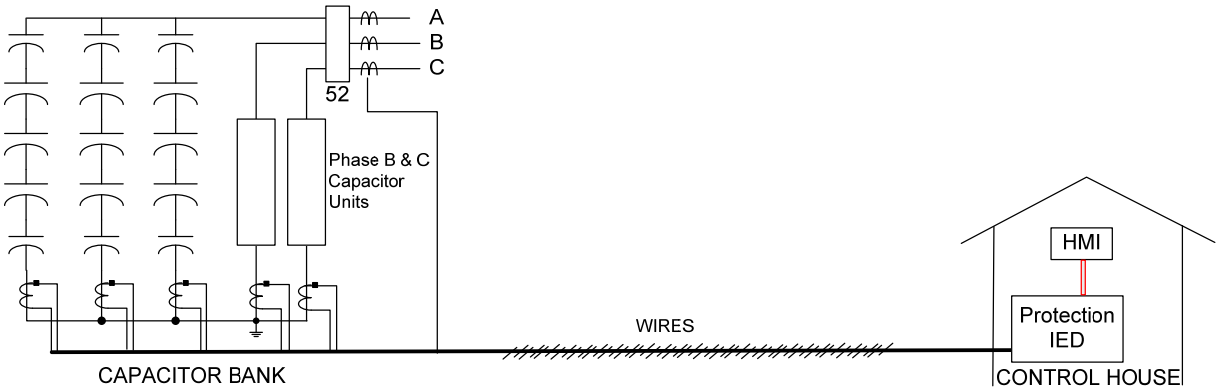
The SOE and DFR data for a 4 string/phase capacitor bank is shown in Table 4. The IED can protect as many as 6 strings. There is more than sufficient to analyze unbalance alarms and trips, and also, arcing fault trips. As new alarms trigger events the new data may be used to evaluate the state of the capacitor bank.

Table 4. SOE and DFR event data for a 4 string/phase capacitor bank

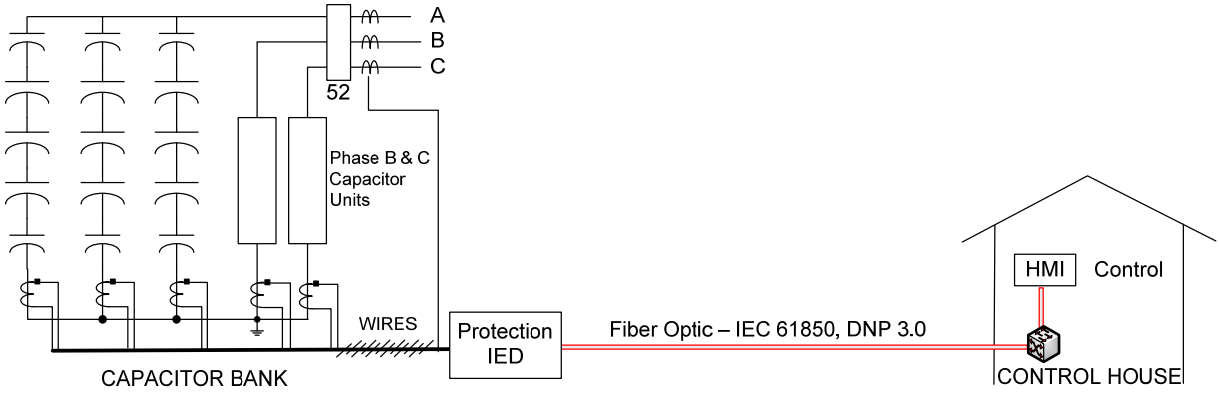
Analog Quantities		**Binary Statuses**			
String Current	**60S Unbalance I**	**Unbalance Alarms**			
Phase A String 1	Phase A String 12	A1L1	A1L2	A1L3	A1L4
Phase B String 1	Phase A String 23	A2L1	A2L2	A2L3	A2L4
Phase C String 1	Phase A String 34	A3L1	A3L2	A3L3	A3L4
3I0 String 1	Phase A String 41	A4L1	A4L2	A4L3	A4L4
Phase A String 2	Phase B String 12	B1L1	B1L2	B1L3	B1L4
Phase B String 2	Phase B String 23	B2L1	B2L2	B2L3	B2L4
Phase C String 2	Phase B String 34	B3L1	B3L2	B3L3	B3L4
3I0 String 2	Phase B String 41	B4L1	B4L2	B4L3	B4L4
Phase A String 3	Phase C String 12	C1L1	C1L2	C1L3	C1L4
Phase B String 3	Phase C String 23	C2L1	C2L2	C2L3	C2L4
Phase C String 3	Phase C String 34	C3L1	C3L2	C3L3	C3L4
3I0 String 3	Phase C String 41	C4L1	C4L2	C4L3	C4L4
Phase A String 4	**Bus Voltage**	**Unbalance Ambiguous Indications**			
Phase B String 4	VA	A12	A23	A34	A41
Phase C String 4	VB	B12	B23	B34	B41
3I0 String 4	VC	C12	C23	C34	C41
	3V0	**Trip Alarms**			
		A1 Trip 1	A2 Trip 1	A3 Trip 1	A4 Trip 1
		B1 Trip 1	B2 Trip 1	B3 Trip 1	B4 Trip 1
		C1 Trip 1	C2 Trip 1	C3 Trip 1	C4 Trip 1
		A1 Trip 2	A2 Trip 2	A3 Trip 2	A4 Trip 2
		B1 Trip 2	B2 Trip 2	B3 Trip 2	B4 Trip 2
		C1 Trip 2	C2 Trip 2	C3 Trip 2	C4 Trip 2

Ethernet and IEC 61850 Application

The protection may be applied conventionally as shown in Figure 12(a). In general, this application is appropriate as long as the cts and their burdens are applied correctly. Considering the availability of new communications technology applying the capacitor bank protection at the capacitor bank location as shown in Figure 12 (b) might be considered. This is one of many possibilities. This can overcome issues related to the small ct burden capability and ct lead length and/or save the considerable cost of the string ct wiring necessary to wire to all of the string cts to the control house.



(a) Conventional application with wiring to IED in control house



(b) IED wired at capacitor bank with optical connection to control house for communicating control and alarm data.

Figure 12. Alternative wiring connections with control and alarm communications

Summary

The relevant aspects of fuseless a capacitor unit, shunt capacitor bank designs and basic concepts of unbalance current protection that are commonly used were reviewed. Using these known protection concepts a new and unique application to detect current unbalanced between capacitor strings and identify the phase and string in which faulted capacitor units are located was presented. The application of string current unbalance protection provides a cost effective method to improve overall protection reliability and the ability to quickly identify and repair faulted strings of the capacitor bank. The grounded bank enables the use of low B.I.L. window type cts that are cost effective. This protection application is based only on current; therefore voltage transformers are not required, making this scheme even more cost effective. To reduce costs further, the implementation of IEC 61850 or DNP 3.0 via fiber can replace the copper ct cable runs, which at the same time reduces the burden on the cts. The application takes into account and solves the issue of ambiguous element failures. The sensitivity of the current measurement is optimized by using a 1A rated current inputs and highly accurate alarm level current measuring units allowing for the required sensitivity to detect only a few failed element series groups.

References

1. IEEE Standard for Shunt Power Capacitors, IEEE Std 18 - 2002
2. IEEE Guide for Application of Shunt Capacitors, IEEE Std 1036-1992
3. IEEE Guide for the Protection of Shunt Capacitor Banks, IEEE Std C37.99-2000
4. IEEE Standard Requirements for Instrument Transformers, IEEE Std C57.13-2003
5. Electrical Transmission and Distribution Reference Book, Chapter 18, page 626, ABB Inc., Raleigh, North Carolina, 1997

Biographies

Elmo Price received his BSEE degree in 1970 from Lamar State College of Technology (Lamar University) in Beaumont, Texas and his MSEE degree in Power Systems Engineering in 1978 from the University of Pittsburgh.

He began his career with Westinghouse in 1970 and worked in many engineering positions that included assignments at the Small Power Transformer Division in South Boston, VA, the Gas Turbine Systems Division in Philadelphia, and T&D Systems Engineering in Pittsburgh. He also worked as a District Engineer located in New Orleans providing engineering support for Westinghouse power system products in the South-central U.S.

With the consolidation of Westinghouse into ABB in 1988 Elmo assumed regional responsibility for product application for the Protective Relay Division. From 1992 to 2002 he has worked at both the Coral Springs, Florida and Allentown, Pennsylvania Divisions in various technical management positions responsible for product management, application support and relay schools. From 2002 to 2008 Elmo was the Regional Technical Manager providing product sales and application support in the southeastern U.S.

Elmo is currently Senior Consultant for ABB and is located in Dawsonville, Georgia. Elmo is a registered professional engineer and a Life Senior member of the IEEE. He is a member of the IEEE Power System Relay Committee and the Line Protection Subcommittee, serving as a contributing member to many working groups. He has two patents and has authored and presented numerous industry papers.

Ryan Wolsey received his BSEE degree in 2006 from the University of Western Ontario in London Ontario, Canada.

He began his career with SaskPower in 2007 in the Protection Design Engineering Department, where he designed protection schemes for new lines and substations.

In 2009 Ryan joined ABB in the Substation Automation Products division in Burlington Ontario Canada and assumed the role of Product and Application Specialist for the North American Market, where he designs protection applications using ABB products.

In 2010 Ryan relocated to ABB Raleigh North Carolina and has continued as the Product and Application Specialist for the North American Market.

Appendix A: Application Example

The following application example is provided to analyze the effects of capacitor element failure and determine appropriate current settings.

Capacitor Bank rating

246.6 kV, 93.6 MVAR three-phase grounded-wye fuseless capacitor bank
3 phase X 48 capacitor units/phase = 144 capacitor units:
Capacitor unit rating: 650 kVAR, 17.8 kV (N = 9 series element groups/unit)
Rated current I_R = 650 / 17.8 = 36.52 A
Each phase: S=8, P=6,

Capacitance and capacitive reactance

$X_C = kV^2 \cdot 1000 / kVAR = 487.45$ per capacitor unit
$C = 1 / 2\pi f X_C = 5.44$ μf per capacitor unit
$C_S = C / S = 0.68$ μf per capacitor string (at rated kV and kVAR values)

Capacitor Element Failure

There are S·N series capacitor element groups per string. When element groups fail (short) the remaining healthy capacitor elements in the string will become overstressed. Assuming operation at rated capacitor bank voltage, the per unit voltage on the healthy capacitor elements, $V_{ELEMENT}$, can be calculated with equation 1.

$$V_{ELEMENT} = \frac{S \cdot N}{S \cdot N - F} \qquad (1)$$

F is the number of failed elements. Table A1 shows the resulting voltages and currents based on the number of failed units F, the capacitor bank rating of 246.6 kV, 93.0 kVAR of 650 and rated string current of 36.52 A.

Current transformer

A 600 V, 10 kV BIL window type ct may be selected for economy. A wound ct having an internal primary winding must be applied with a higher voltage rating per reference [3], but will be considerably more expensive. The primary ct rating should be selected to be higher than the rated string current and provide a secondary current of 1 to 3 amps and must have suitable burden. For this application a 100/5 ct with a C10 rating is selected. The rated string current will be 36.62 A primary and 1.83 A secondary.

Table A1 Failed Capacitor Element Group Analysis

Failed Elements	Ohms	kV per Element	Vpu on Remaining Elements	String Current	I Unbal Primary A	I Unbal Secondary A	String Current Unbalance in % of Rated
0	3899.57	1.9778	1.00	36.52	0.000	0.00	0.00%
1	3845.41	2.0056	1.01	37.03	0.514	0.03	1.41%
2	3791.25	2.0343	1.03	37.56	1.043	0.05	2.86%
3	3737.09	2.0638	1.04	38.10	1.588	0.08	4.35%
4	3682.93	2.0941	1.06	38.66	2.148	0.11	5.88%
5	3628.77	2.1254	1.07	39.24	2.725	0.14	7.46%
6	3574.61	2.1576	1.09	39.84	3.320	0.17	9.09%
7	3520.44	2.1908	1.11	40.45	3.933	0.20	10.77%
8	3466.28	2.2250	1.13	41.08	4.565	0.23	12.50%
9	3412.12	2.2603	1.14	41.73	5.217	0.26	14.28%
10	3357.96	2.2968	1.16	42.41	5.890	0.29	16.13%
11	3303.80	2.3344	1.18	43.10	6.585	0.33	18.03%
12	3249.64	2.3733	1.20	43.82	7.303	0.37	20.00%
13	3195.48	2.4136	1.22	44.56	8.046	0.40	22.03%
14	3141.32	2.4552	1.24	45.33	8.814	0.44	24.14%
15	3087.16	2.4982	1.26	46.13	9.610	0.48	26.31%
16	3033.00	2.5429	1.29	46.95	10.433	0.52	28.57%
17	2978.84	2.5891	1.31	47.80	11.287	0.56	30.91%
18	2924.68	2.6370	1.33	48.69	12.172	0.61	33.33%
19	2870.52	2.6868	1.36	49.61	13.091	0.65	35.85%
20	2816.36	2.7385	1.38	50.56	14.045	0.70	38.46%
21	2762.19	2.7922	1.41	51.55	15.036	0.75	41.17%

Settings

k_{XJ} string current balancing factor

Generally the capacitor bank is provided with capacitor units distributed in the bank to balance phase and string capacitance to within 0.5% and balancing string current is not be needed. The unit rated capacitance plus the tested deviation per Table 2 of each unit may be used to calculate and verify unbalance prior to bank energization. Also, once energized the individual string currents should be monitored to verify.

The k_{XJ} factor allows adjusting each string ct ratio individually at commissioning to set primary current as measured by the relay to a common value such that all the digital string primary values are very nearly equal (i.e. $I_{A1} = I_{A2)} = I_{A3} = \ldots = I_{AP}$) eliminating the inherent unbalance due to manufacturing tolerance. The k_{XJ} factor is implemented by modifying the CT_P ratio settings. Assume the measured string capacitance [or measured current] values of phase A at commissioning are as shown in Table A2.

Consider that the string capacitance values run about 6% on the average above rated, which is not unexpected. Also, consider that when the capacitor bank is energized it may be operating a system voltage different than the bank rating. Therefore the measured current will be different from rated.

Table A2. k_{XJ} values for 6 strings of phase A adjusted to string 3 measured primary current

String Number (J)	1	2	3	4	5	6
Rated C_S μf	0.68					
Measured C_S μf	0.715	0.725	0.721	0.727	0.717	0.719
Rated Current	36.52					
Measured I @ 230kV	35.8	36.25	36.1	36.4	35.9	36.0
K_{AJ}	1.008	0.996	1.00	0.992	1.006	1.003
CT Primary Settings	202	199	200	198	201	201
Compensated I	36.16	36.07	36.1	36.04	36.08	36.18

Using a the measured value of either string capacitance, C_N, or string current, $I_{N,}$ of a reference string, the k_{XJ} value can be computed for all strings in all phases. For this example string 3 is selected as the reference value, either current or capacitance, as it is close to the median of the bank measured values. A 100/5 ct is being used; however, the ct primary/secondary settings, which are set as integers, will be set at nominally 200/10 to provide better compensation resolution for the k_{XJ} value. For each string the following computations are made. The results are shown in Table 4 with not more than 0.28% unbalance between strings.

$$k_{AJ} = \frac{C_N}{C_{(AJ)MEASURED}} = \frac{I_N}{I_{(AJ)MEASURED}}$$

$$CT_{(AJ)PRI-SETTING} = Int\left(k_{AJ} \cdot 200\right)$$

$$I_{(AJ)COMP} = I_{(AJ)MEASURED} \cdot \frac{CT_{(AJ)PRI-SETTING}}{200}$$

It is desirable that the measured string capacitance values be used to calculate the k_{XJ} factors and apply the compensation before the capacitor bank is energized. This will assure minimum unbalance when the bank is energized and verification is made comparing the now compensated primary currents. This might be impractical; therefore, compensation with measured currents at commissioning is appropriate given the little unbalance expected. Note that this example shows the compensation for only one phase and that there should be only one nominal value used for the entire bank.

Unbalance current settings

Settings are made in primary values, either amps or as a percent of a base value. In this case the rated string current of 36.62 A is used as the base value and all the settings are expressed as a percent of this base value. The per unit voltage on remaining capacitor element groups and the corresponding % unbalance current as a function of the number of failed element groups are shown in the Table 3.

Selected alarm and trip pickup and time delay values are shown in Table A3. Alarms 1, 2 and 3 are set to provide early warnings of element failures. The 4 second time delay is rather arbitrary and is set at this value to assure measurement stability and avoid false alarming. Alarm 4 and Trip is set at 10% of rated string current with a 2 second trip delay. Again this time delay is longer than normal tripping as it is only concerned with internal capacitor element failures and does not consider arcing faults. The time delay should coordinate with the slowest clearing case of system faults.

Table A3. Current Unbalance Settings

Condition	I pickup % of Rated String Current	Time delay (seconds)	Comments
60S-A and 60N-A (Element failure alarms and trip)			
Alarm 1	2.5	4	Low level – 2 failed element groups
Alarm 2	5.0	4	Mid level – 4 failed groups
Alarm 3	7.5	4	Upper mid level – 5 failed groups
Alarm 4 & Trip	10.0	2	High level – 7 failed element groups. Unbalance trip
60S-T and 60N-T (Arcing fault and excessive element failure fast trips)			
Trip 1	13.5	0.1	Trip level 1 – 1 capacitor unit is shorted due to arcing faults or 9 element failures
Trip 2	20.0	0.05	Trip level 2 – more than one capacitor unit is shorted due to arcing fault or 12 element group failures

Trip 1 and Trip 2 are for fast tripping of external arcing faults and rapid escalation of internal capacitor element faults. Trip 1 is set to trip for one capacitor unit [or 9 element groups] being shorted and Trip 2 is set to detect more than one unit [or 12 element groups] being shorted. The Alarm 4 Trip, Trip 1 and Trip 2 coordination with the capacitor overcurrent limit for fundamental frequency current is shown in Figure A1. The curve was developed from the fundamental frequency momentary overvoltage limit for capacitors.

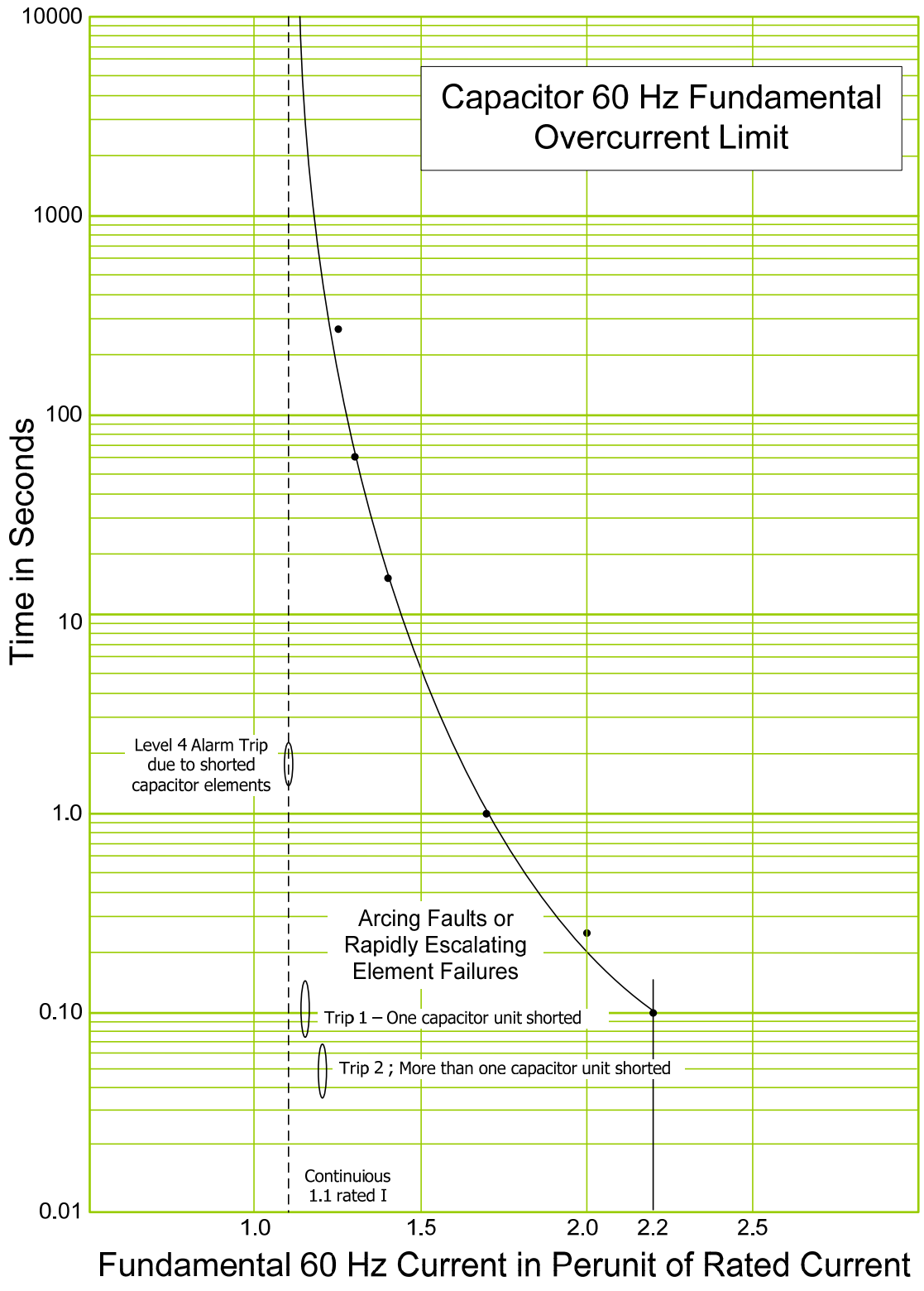


Figure A2. Capacitor fundamental overcurrent capability based on IEEE C37.1036 overvoltage capability defined in Table 1 with coordinated trips