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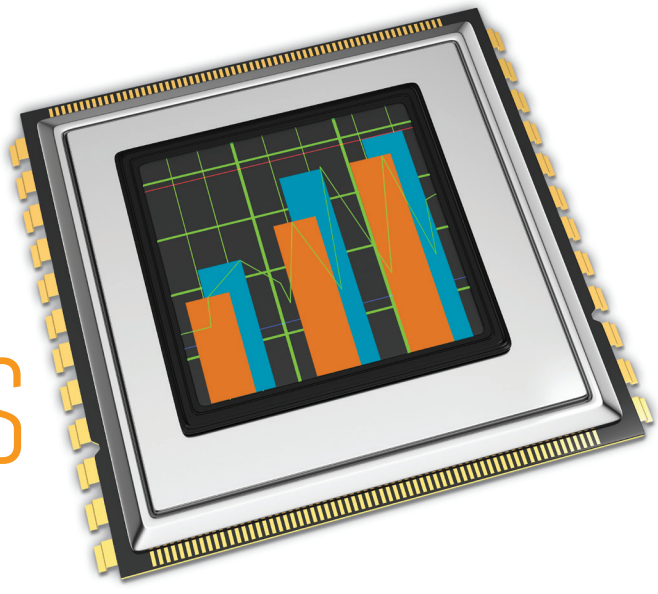
FAB-WIDE EFFORT INCREASES YIELD



AT CMOS IMAGER FACILITY IN ITALY

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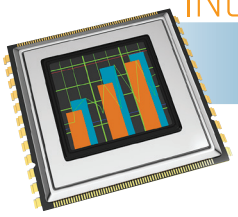
A CASE STUDY

Manufacturers must continually refine and improve their operations in order to meet increasingly difficult device performance and yield goals. This article describes a fab-wide engagement in which Applied Materials' FabVantage consulting group helped one customer solve a variety of yield challenges across a fleet of tools. The result has been a significant and sustainable increase in the fab's overall yield.

APPLIED MATERIALS®



FAB-WIDE EFFORT INCREASES YIELD AT CMOS IMAGER FACILITY IN ITALY

The goal of Applied's FabVantage consulting group is to help customers increase their operational capability with respect to cost, efficiency and yield. FabVantage consultants address customer productivity and yield issues by combining the skills and knowledge of seasoned fab experts with state-of-the-art modeling and analysis tools, and Applied's deep systems and technology roots.

A good example of the benefits of this collaboration are the results of an extensive fab-wide engagement encompassing about 10 separate projects that took place at a CMOS image sensor array fab in Avezzano, Italy. The fab is run by Marsica Innovation & Technology srl (MIT), an operating company of the joint venture between LFoundry Europe and Marsica Innovation SpA.

For each of 12 tool-types, the team audited tools and recipes, and used sensor- and on-wafer data to pinpoint key issues. By leveraging best known practices and specific expertise, the team made recommendations to improve performance. In most cases, proposed solutions were first tested on a golden tool. Successful solutions then were fanned out to the entire fleet. As the work progressed, the team evaluated not only individual chambers and tools, but also looked at some aspects of production from a more integrated perspective, examining several tools that together were engaged in carrying out specific process steps.

Here are a few examples showing how yield improvements were achieved.

MODIFIED ETCH PROCESS REDUCES DEVICE LEAKAGE

On one etch tool, excessive transistor current leakage was observed following an oxide spacer etch step. When fab personnel tried to address the problem through preventive maintenance and auto-cleanings, the leakage became even worse.

A detailed recipe and process audit was initiated. The FabVantage team determined the root cause of the problem to be a recipe with low oxide-to-polysilicon sensitivity, which sometimes led to over-etching into the silicon substrate. Further complicating the matter, this over-etching was not uniform across the tool's chambers.

Applied and the customer identified an optimized recipe as the best solution (see figure 1). It was also determined that the chamber lid temperature set point varied from chamber to chamber, which caused nonuniform etching across chambers. In addition, sensor trace analysis and Applied's best known methods (BKMs) were used to optimize the etch process to eliminate voltage spikes that are known to lead to yield loss.

BETTER CONTROL OF VARIABILITY IN RTP PROCESS

Elsewhere, there was significant variability in the performance of a rapid thermal processing (RTP) tool at a new technology node, with resulting transistor performance issues across wafers.

Audits of hardware, maintenance practices, process recipes, and fault detection and classification (FDC) analyses identified the tool's temperature profile as the root cause of the process variability. Excessive temperatures during ramp-up turned out to be the specific cause of the transistor performance problems. Additionally, the team found other temperature issues that impacted the tool's ability to achieve targeted yields. These were excessive temperature differences among heater zones during the stabilization phase of the process, and poor temperature control during spike anneal.

Temperature overshoots during ramp-up caused oxide growth and dopant out-diffusion, and these effects led to the variation in device performance. In response, the customer and the FabVantage team modified the tool's system controller to optimize it for the temperature ramp-up step (see figure 2a).

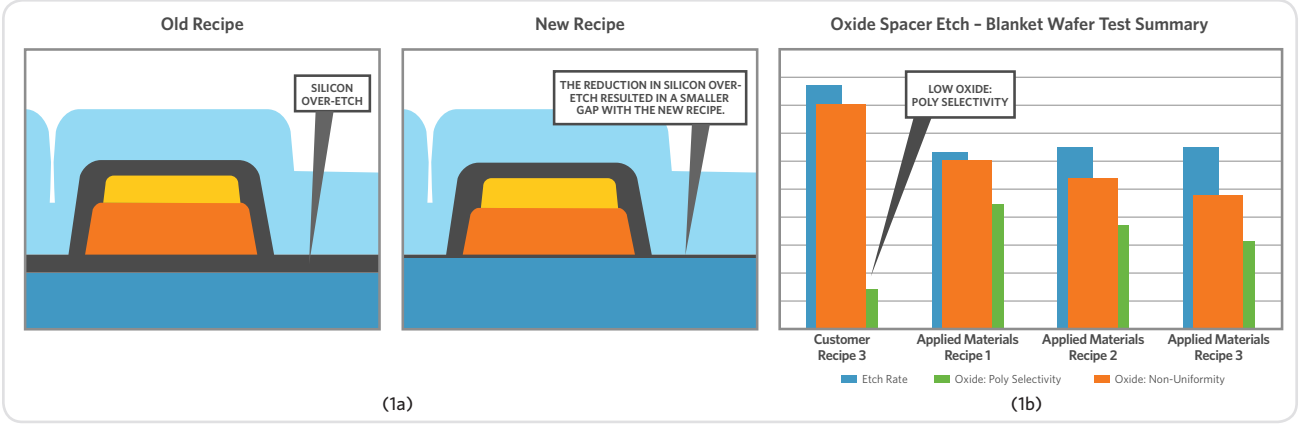


Figure 1. A recipe with low oxide-to-polysilicon sensitivity sometimes led to over-etching into the silicon substrate (figure 1a left). A new recipe eliminated the problem (figure 1a right). The graph compares the oxide-to-polysilicon sensitivity of several of Applied's proposed recipe changes with the customer's original recipe (figure 1b).

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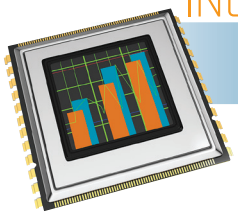
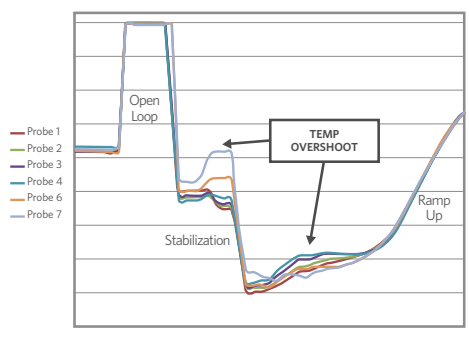
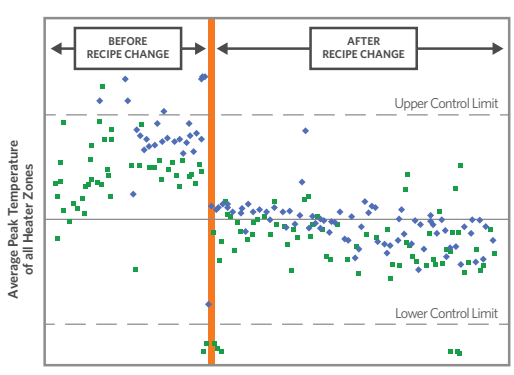


Meanwhile, the recipe audit identified chamber pressure as a cause of peak temperature control issues, and the recipe was modified to accommodate higher pressures (see figure 2b). Finally, hardware/maintenance practice audits revealed that the tool's process kit was marginal, and also that preventive maintenance procedures needed to be optimized. The hardware issues were addressed and BKM cleaning procedures were implemented.



(2a)



(2b)

Figure 2. An RTP tool's system controller was optimized to eliminate temperature overshoots during ramp-up (figure 2a). These can cause oxide growth and dopant out-diffusion, and lead to variations in transistor performance across wafers. Also, the beneficial effects of a recipe change to accommodate higher chamber pressures are shown in figure 2b. The FabVantage team discovered that chamber pressures were causing peak temperature control issues. The new recipe led to more uniform temperatures across heater zones.

DEFECT REDUCTION LEADS TO BETTER CMP

A chemical-mechanical planarization (CMP) tool was unable to achieve targeted yields because of scratches generated during a polishing step. These scratches were being generated at more than three times the number that could be tolerated by the customer's technology.

The FabVantage team conducted several tool audits to understand the problem and identify solutions. They determined that upstream processes induced particles at the wafer edge that subsequently scratched the wafer during polishing. A multi-faceted solution was recommended and implemented that focused on optimizing slurry delivery, evaluating specific tool components, and conducting upstream preventive maintenance activities in accordance with Applied's BKMs. The result was a more than 300% reduction in scratches (see figure 3).

IMPROVED PROCESS STABILITY

Production and yields from a PVD tool that was trying to run a new recipe were impacted by the complexity of a cobalt silicide (CoSi) deposition loop, which led to widespread transistor leakage and logic timing failures during wafer probe tests.

The FabVantage consultants determined that failures were dependent on product-type, process integration of the CoSi step was marginal, and within-wafer leakage patterns were related to the thickness of the cobalt film—the thicker the Co, the worse the leakage.

The team recommended improved inline electrical parametric tests and test layouts as a way to detect failure mechanisms early, as well as the implementation of a very soft sputter (VSS) etch process prior to Co deposition to improve film uniformity (see figure 4). Modifications to pressure and power to improve process stability were suggested, and the Co PVD recipe was optimized for better within-wafer and wafer-to-wafer thickness uniformity.

OPTIMIZED ALUMINUM DEPOSITION REDUCES HILLOCKS

One PVD tool was experiencing yield loss with specific device-types because high aluminum (Al) hillocks were being produced by the baseline process. Although the customer had implemented a patch to contain the problem, it was costly.

These hillocks were caused by Al film stress, which can be modulated by the temperature of the hot Al deposition step. However, a lower Al de-gas temperature can lead to defects in subsequent steps; therefore a number of related processes need to be tuned in accordance with changes in Al deposition.

A series of changes to the stack recipe were recommended and implemented, from de-gas to Al reflow, which reduced the number of hillocks by more than half. The results were validated by electrical parametric tests (see figure 5).

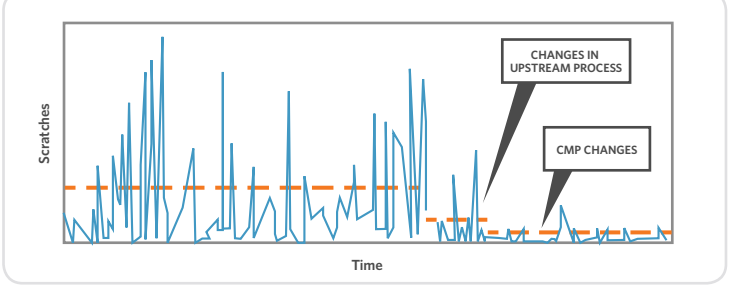


Figure 3. Tool audits conducted by the FabVantage team led to a more than 300% reduction in scratches from one CMP tool. The team recommended changes to upstream preventive maintenance procedures in accordance with Applied's BKMs, and optimized slurry delivery and evaluation of certain tool components.

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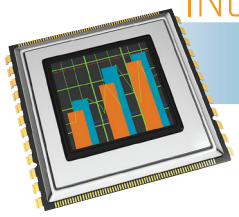

TOOL AVAILABILITY IMPROVEMENT

Other results of the work performed during the fab-wide consulting engagement include:

- **Greater Availability.** The uptime and stability of one PVD tool used to fabricate copper barrier/seed (CuBS) layers was increased by the addition of a new bell jar component. DC bias deterioration was eliminated and RF matching for load and tune positions was stabilized.
- **Backside Etch Defect Reduction.** One Applied Centura tool was experiencing intermittent yield loss from defects during backside etch. FabVantage consultants identified chamber maintenance practices as the root cause of the defects. They then recommended and helped implement new procedures for electrostatic chuck (ESC) cleaning and inline defect detection.
- **Side-to-Side Chamber Mismatch Eliminated.** The parameters of devices produced on different sides of one Applied Producer CVD tool's chamber were mismatched. The team determined the tool's showerhead was one factor; the second factor was differences in the level of radio frequency (RF) power from one side to the other. A faceplate change at the next preventive maintenance cycle was recommended, and the level of RF power applied throughout the chamber was optimized and equalized.

The key to successful semiconductor manufacturing is to achieve and maintain the highest possible yields at the lowest possible cost. As this project demonstrates, well-qualified and experienced consultants such as those in Applied's FabVantage group, backed by extensive technology resources, can help manufacturers achieve those goals.

Acknowledgements:
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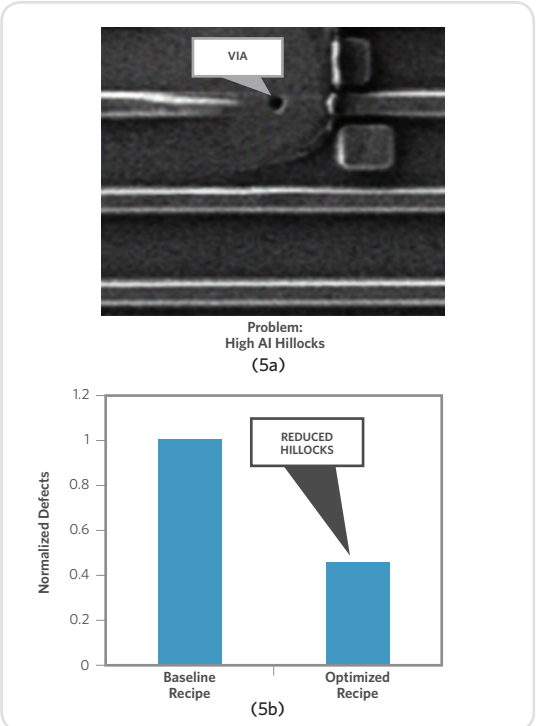

Figure 5. The Al hillocks seen at left were caused by Al film stress and were impacting yields from a PVD tool (figure 5a). Applied's FabVantage consultants recommended a number of ways to reduce film stress, reducing hillock formation by more than half (figure 5b).

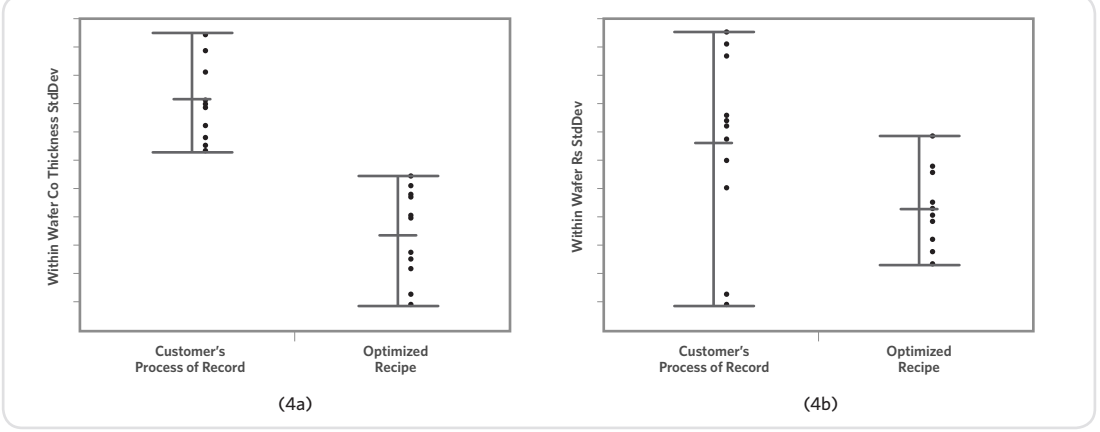

Figure 4. Tool hardware and recipe audits of tools in the CoSi loop uncovered several findings that were contributing to poor transistor performance. After optimizing the Co PVD recipe to eliminate transient steps and increase pressure and power, the standard deviation of within-wafer thickness uniformity decreased by almost half (figure 4a) and the standard deviation of within-wafer resistivity declined about 15% (figure 4b). More importantly, resistivity was controlled in a tighter range.