

DATA-CENTRIC HPC MINIMIZING DATA IN MOTION

DELL Accelerating Understanding Summit May 31 –June 1, 2016 Paris, France

Herbert Cornelius Intel Corporation

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Notice revision #20110804



INDUSTRIAL REVOLUTION 4.0

1.0

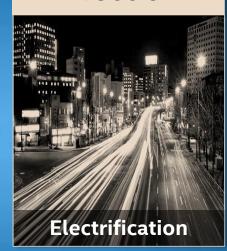
Steam

1760's

Coal
Railways
Factories
Printing Press
Mass Education

2.0

1860's



Communication,
Oil, Combustion Engine
New materials
Highways, Automobiles
Mass Production

2000's

seen. When I was and the track was and the track was and the track was and the track was and the track.

WWW
Molecular Biology
Green Energy
Mobility
Automation

Digitization

4.0 FUTURE VISION 2020's



Cloud Computing
Super Information Data Highways
Industrial Internet, M2M
Internet of Things (IoT)
Smart "everything"
Personalized Medicine
Big Data (Analytics) & AI

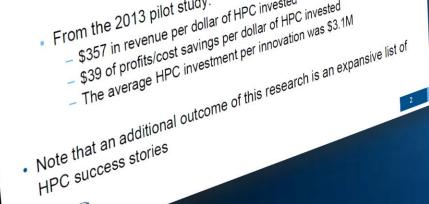


New Findings: The ROI Is Very High

New results indicate higher ROI returns related to investments in HPC, compared to the pilot study

- On average, from the latest data:
 - \$514.7 in revenue per dollar of HPC invested
 - \$43.2 of profits/cost savings per dollar of HPC invested The average HPC investment per innovation was \$3.0M
- \$357 in revenue per dollar of HPC invested From the 2013 pilot study:

 - \$39 of profits/cost savings per dollar of HPC invested





1 hpcuserforum.com/presentations/Colorado-sept2015/PublicIDCDOEROIResearchUpdate8.19.2015.pdf ² www.hpcwire.com/2014/01/02/top-supercomputing-discoveries-2013



IDC Andreas

TRANSFORMATION & DEMOCRATIZATION

HIGH-PERFORMANCE COMPUTING

1970's CRAY-1



Proprietary

1990's ASCI RED



Industry Standards

2010's KNIGHTS LANDING**



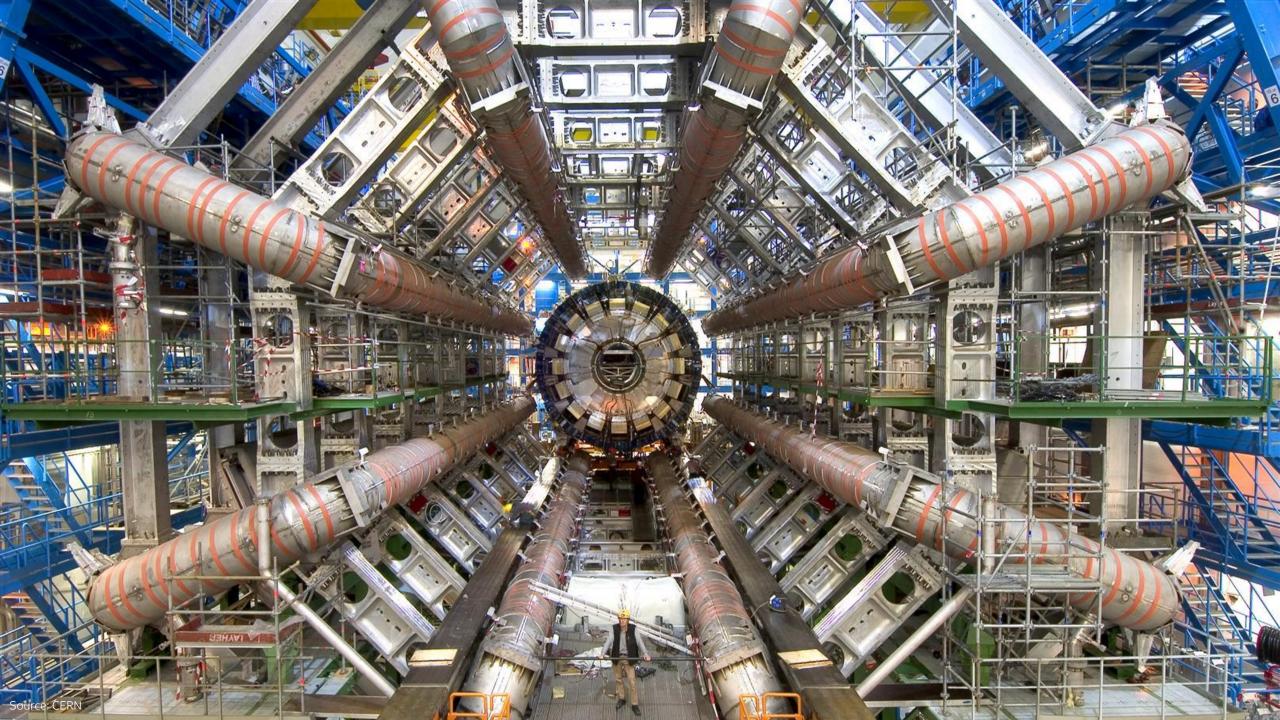
Miniaturization

**For illustration only, not drawn to scale. Potential future options are forecasts and subject to change without notice.



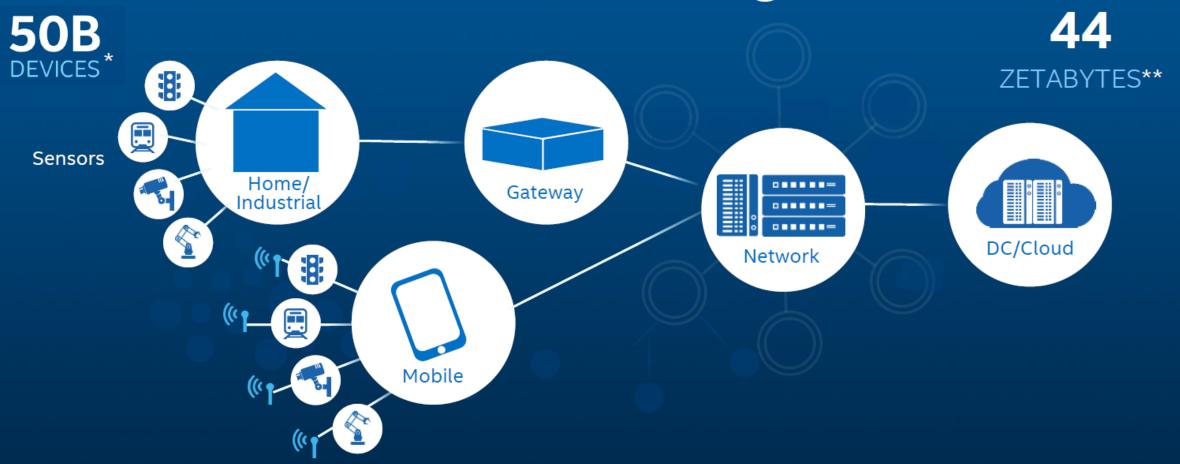


DATA IS EXPLODING





The Internet of Things is...



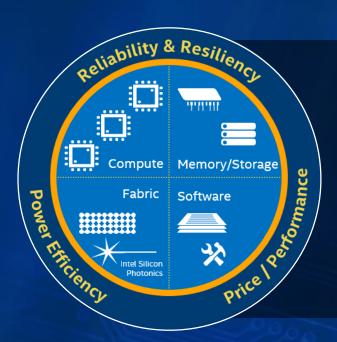








A HOLISTIC DESIGN SOLUTION FOR HPC INTEL® SCALABLE SYSTEM FRAMEWORK (SSF)



Small Clusters Through Supercomputers

Compute and **Data-Centric** Computing

Standards-Based Programmability

On-Premise and Cloud-Based

Tighter Integration

Intel® Xeon® Processors

Intel® Xeon Phi™ Processors

Intel® Xeon Phi™ Coprocessors

Intel® Server Boards and Platforms

Intel® Solutions for Lustre*
Intel® SSDs
Intel® Optane™ Technology
3D XPoint™ Technology

Intel® Omni-Path Architecture
Intel® True Scale Fabric
Intel® Ethernet
Intel® Silicon Photonics

HPC System Software Stack
Intel® Software Tools
Intel® Cluster Ready Program
Intel® Visualization Toolkit



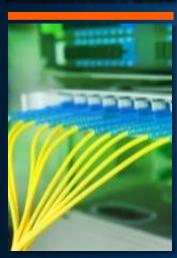
NEW INTEL TRANSFORMING HPC & BIG DATA





COMPUTE

ARCHITECTURE



FABRIC

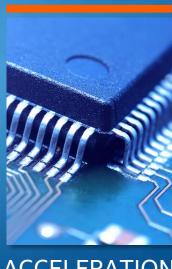


I/O



MEMORY STORAGE

FPGAS

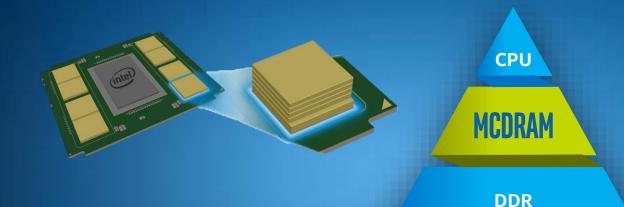


ACCELERATION



HIGHLY PARALLEL PROCESSING

KNIGHTS LANDING **NEXT-GEN INTEL® XEON PHI™ PROCESSOR**





VS. KNC

FASTER MCDRAM VS. **DDR4 DIMMs** **SSDs**

Hard Disk Drives



For illustration only. All dates, product descriptions, features, availability, and plans are forecasts and subject to change without notice.

3D XPOINT™ TECHNOLOGY (NVM)

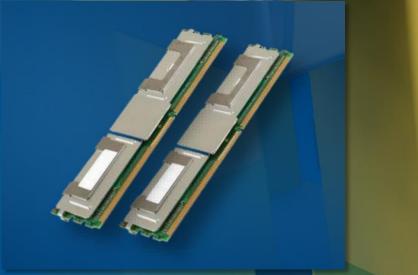
INTEL® OPTANE™ SSD



NEW CLASS OF NON-VOLATILE STORAGE

10x faster than NAND
1000x endurance of NAND

DIMMs** BASED ON 3D XPOINT™



NEW CLASS OF NON-VOLATILE MEMORY**

4x more memory capacity

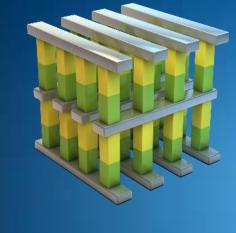
1/2 cost of DRAM

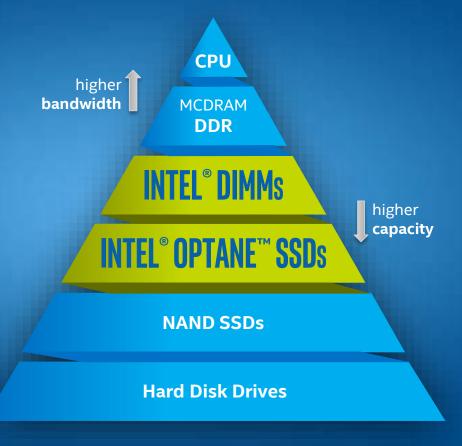
**For illustration only, future potential options are forecasts and subject to change without notice.



NEW MEMORY & STORAGE

3D XPOINT™ TECHNOLOGY





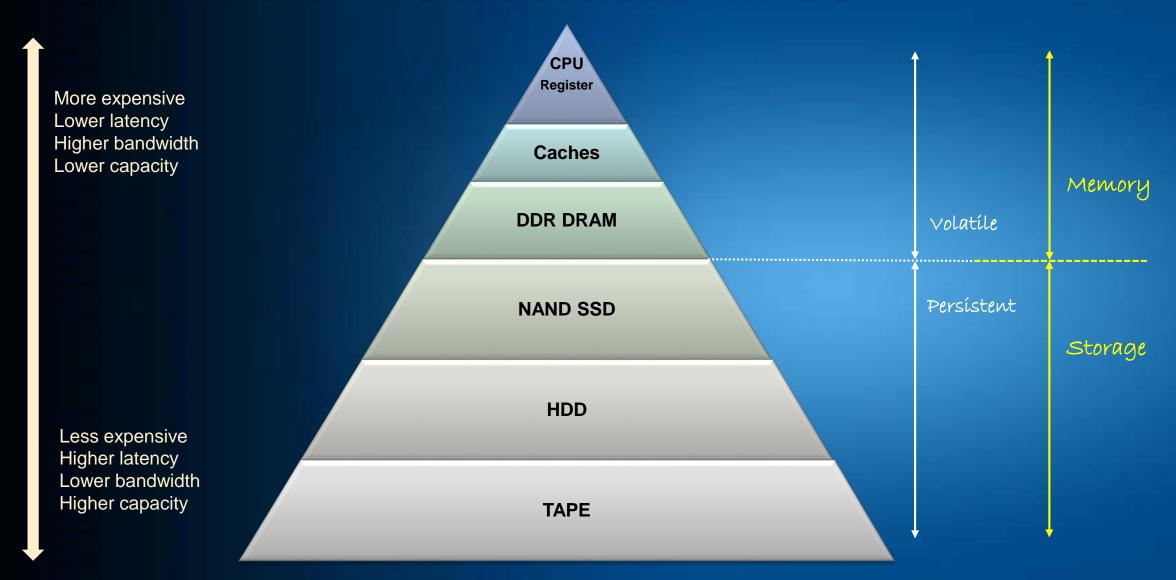
10X FASTER THAN NAND (LATENCY)

1000X ENDURANCE OF NAND

10X DENSER THAN DRAM



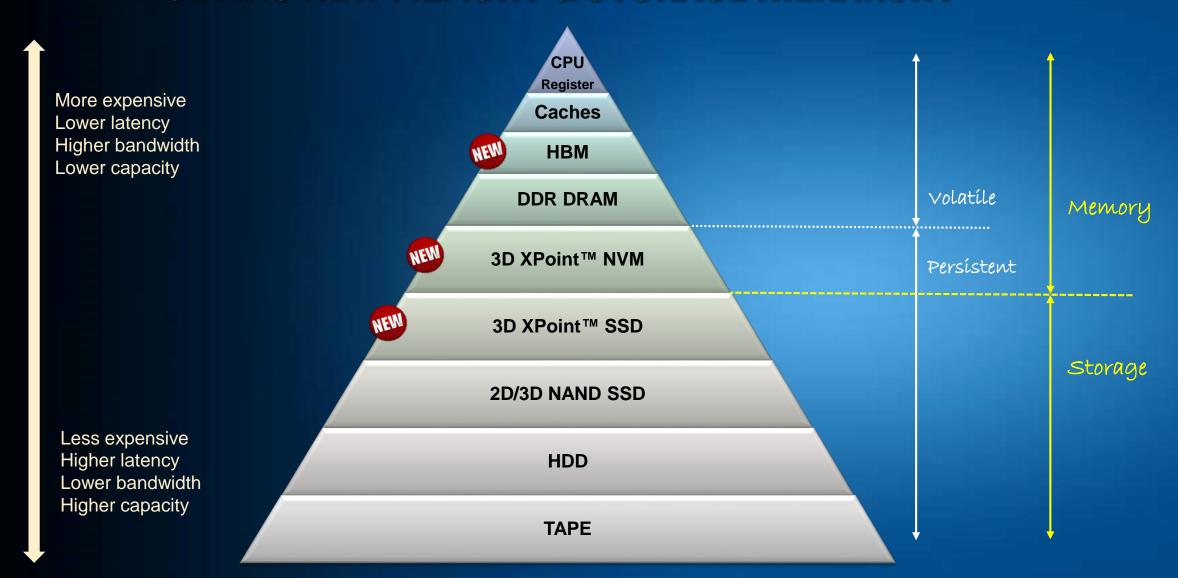
TODAY'S MEMORY & STORAGE HIERARCHY



For illustration only, not drawn to scale



EVOLVING NEW MEMORY & STORAGE HIERARCHY



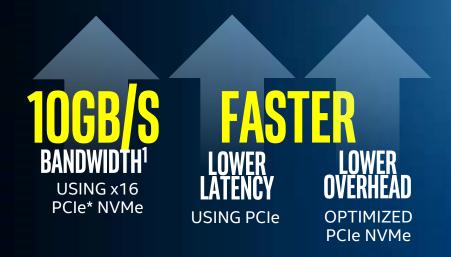
For illustration only, not drawn to scale

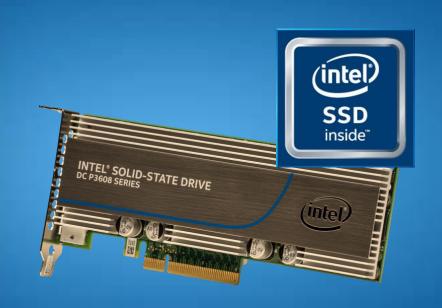


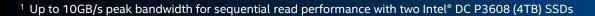
MAKING STORAGE FASTER

High Performance . Efficiency . Reliability . Consistency

INTEL® SSDs 2D/3D NAND



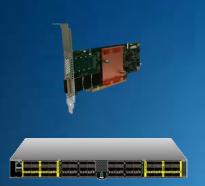






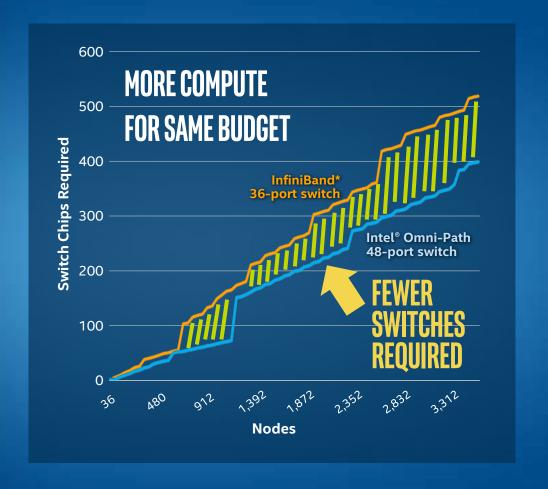
THE NEW HPC FABRIC

INTEL® OMNI-PATH™ ARCHITECTURE



100
GBIT/S
PER SWITCH DENSITY

2.3X
GREATER
FABRIC
SCALABILITY

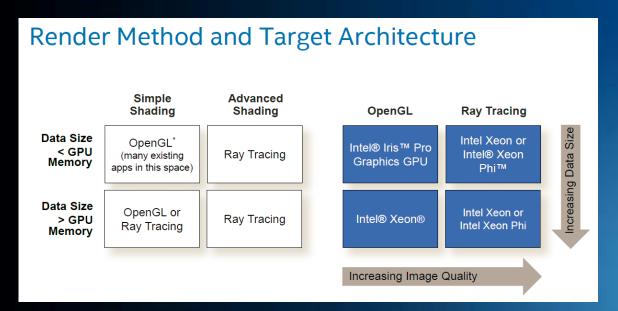


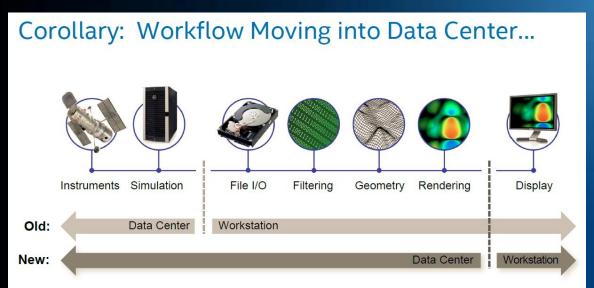
Number of switch chips required, switch density, and fabric scalability are based on a full bisectional bandwidth (FBB) Fat-Tree configuration, using a 48-port switch for Intel® Omni-Path Architecture and 36-port switch ASIC for either Mellanox* or Intel® True Scale Fabric. *Other names and brands may be claimed as the property of others. 2.3X fabric scalability based on a 27,648-node cluster configured with the Intel® Omni-Path Architecture using 48-port switch ASICs, as compared with a 36-port switch chip that can support up to 11,664 nodes.

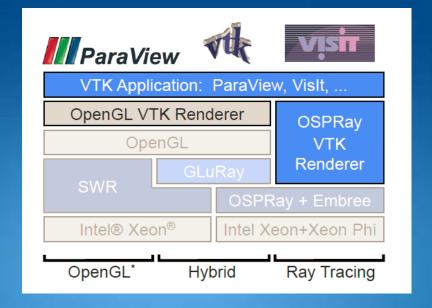


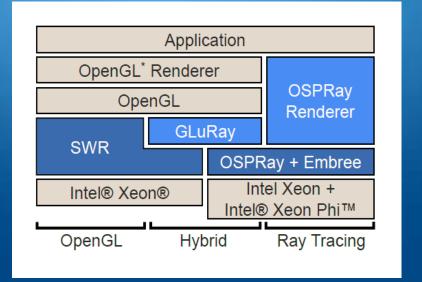


HIGH FIDELITY VISUALIZATION: IN SOFTWARE - IN SITU













MODERN CODE DEVELOPER COMMUNITY

software.intel.com/en-us/modern-code

INTEL CODE MODERNIZATION PROGRAM

software.intel.com/en-us/code-modernization-enablement

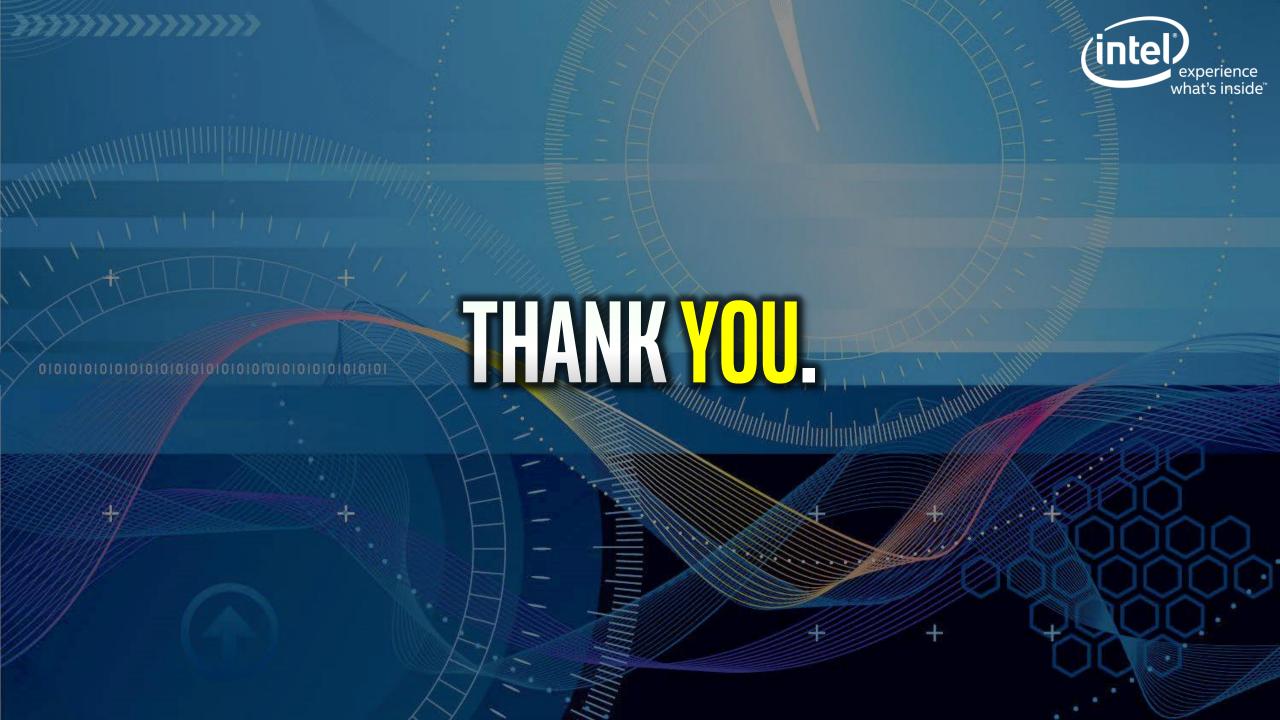
INTEL PARALLEL COMPUTING CENTERS

software.intel.com/en-us/ipcc

INTEL PARALLEL UNIVERSE MAGAZINE

software.intel.com/en-us/intel-parallel-universe-magazine





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Rev. 4/15/14

