

POWER STRUGGLE:

AS MOBILE SYSTEMS OFFER
ADDITIONAL MEMS SENSORS,
POWER IS A PRIMARY CHALLENGE

**BY
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To be sure, we can all look forward to an array of exciting new capabilities built into everything you can imagine—from cars and smartphones to intelligent appliances and wearable technology—based on a range of new sensors and ICs (see figure 1). The behind-the-scenes challenge, however, is to deliver power to those components without exceeding the system’s power budget. That is spurring power IC vendors to develop new device architectures and advanced 200mm manufacturing techniques.

Jeremie Bouchaud, senior principal analyst for MEMS and sensors at market research firm IHS, said environmental sensors on the horizon will turn smartphones into “micro gas chromatographs” able to monitor pollen in the air or alcohol on one’s breath. STMicroelectronics foresees each phone having a micro display capability. Apple’s decision to provide a fingerprint MEMS sensor in its latest iPhone will soon be emulated by the Android smartphone camp.

As more sensors are added, consumers are keeping one eye on the battery’s charge level. Partly to keep power under control, the iPhone5 includes a dedicated coprocessor to handle the fingerprint processing and other data streams coming from MEMS devices. And with Intel Corporation squarely behind the trend, smartphone and mobile computer users soon may be able to take advantage of wireless charging; for example, drivers may be

able to lay a smartphone down on the car’s center console to charge the battery.

Other developing—and potentially huge—markets for power semiconductors include solar-powered buildings and battery-powered electric vehicles, which depend on efficient high-voltage power-switching ICs. Home appliances and HVAC systems are fertile markets for smarter power electronics (see figure 2).

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Rob Lineback, an IC Insights analyst who tracks power ICs as part of the market research firm's report on optoelectronics, sensors, and discretes (O-S-D), said much of the attention in the power field has been on mobile systems, principally smartphones. "Battery power management has been talked about for so long. But there is renewed attention on reducing the power consumption of the big computers and switches, partly so we can cut air pollution from the power plants. Power management plays across the whole range of systems, and there is a lot of money there for the semiconductor companies."

The consolidation in the chip industry, so Darwinian for makers of memory and digital ICs, has not impacted the power IC market as severely. Lineback noted that while

Japan-based companies have cut back on investments in system-on-chip production, "they keep investing in the power area. No one is selling off or consolidating in this area."

Market research firm Yole Développement predicts 19.5% growth for the power electronics market—including power ICs, power modules, and discretes such as rectifiers—with total revenues for the sector approaching \$14 billion. Revenues for power ICs by themselves will increase from \$3 billion in 2013 to about \$3.55 billion in 2014. By 2018 power electronics will be a \$16 billion sector, the market researcher predicts, with power ICs accounting for \$4.23 billion of the total.

In a 2013 study of the super junction (SJ) power IC market, Yole noted that several new players entered the SJ MOSFET market over the last 36 months, including some smaller

foundries in China, raising the number of competitors to about 15. "We have seen new business models emerge, and unexpected players entering," Yole concluded.

For a variety of technical reasons, SJ power ICs are gaining acceptance compared with conventional power MOSFETs, particularly in consumer applications such as phones and tablets. With their high aspect ratio (HAR) trenches, SJ MOSFETs can be much smaller than lateral or planar power MOSFETs, with faster switching speeds due to a lower ON resistance. Though SJ MOSFETs can also be used in relatively high-power applications, the architecture excels in the small power supplies used in mobile systems that must stay within a relatively low operating temperature range. Vendors are reducing the die sizes of SJ offerings, and smaller packages also are coming to the market.

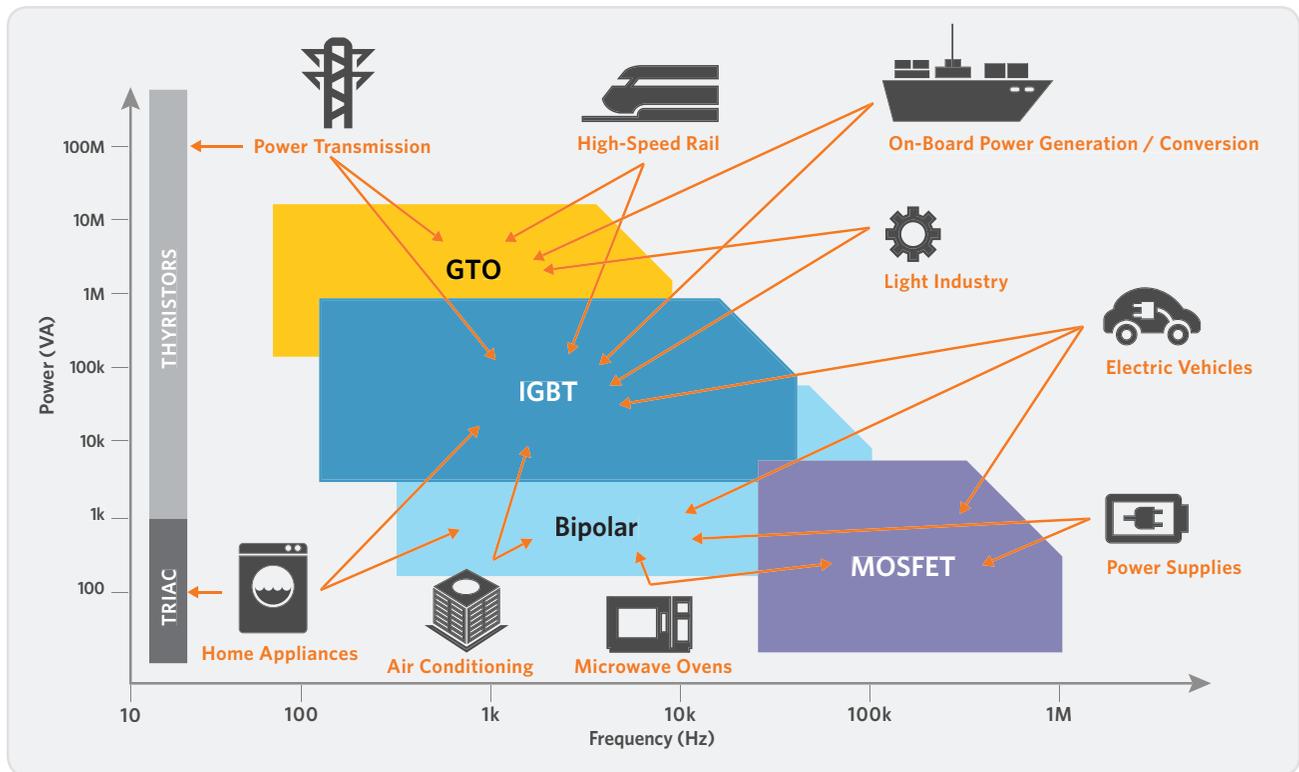


Figure 1. Today's advanced power switching applications are driven mostly by the fast-growing consumer market. While higher frequency and ever higher power-handling capabilities are sought, portability is also a key factor because there is increasing pressure to make these devices smaller and more efficient. In doing so, the device density increases and so does the complexity of manufacturing for this class of semiconductor power device. (Courtesy of Yole Développement.)

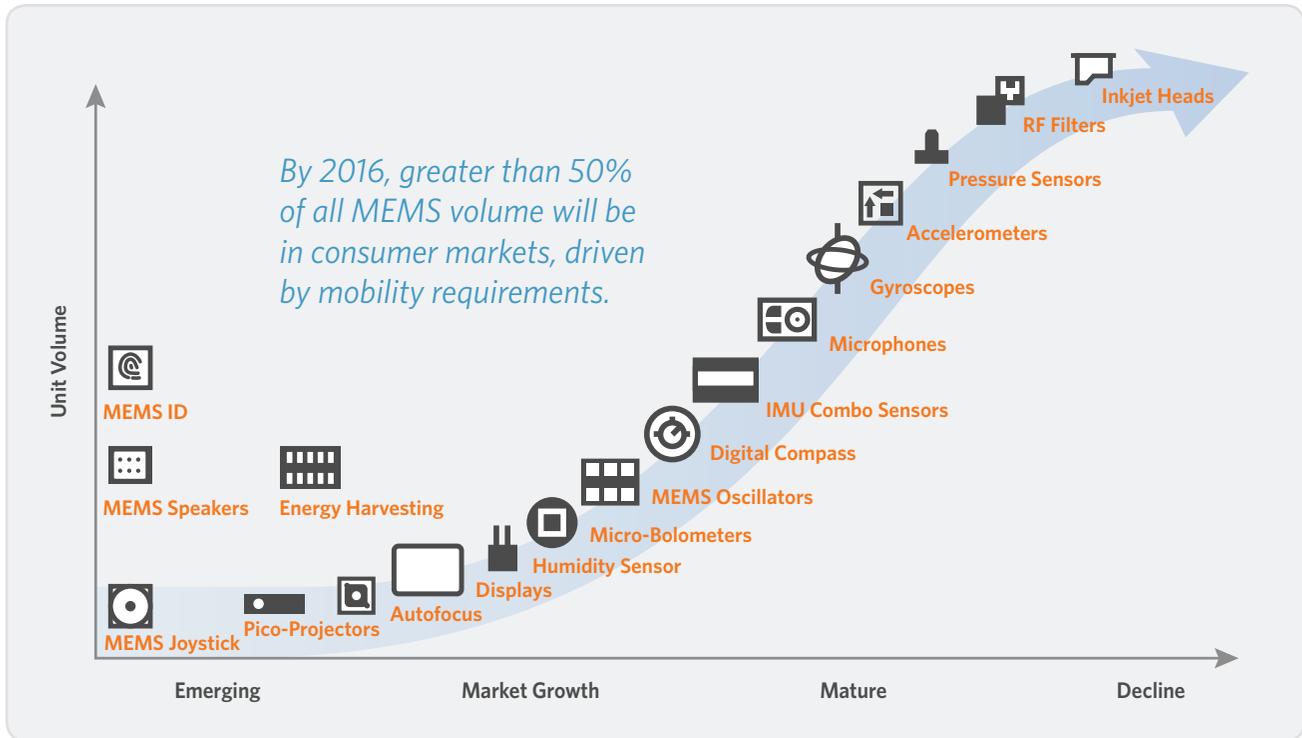


Figure 2. The push for more functionality in portable electronics has resulted in more MEMS technology with each generation of consumer device. Some MEMS devices, such as the Inkjet, are mature; others, such as the inertial measurement unit (IMU) combo sensor, are in a high-growth phase. Devices such as pico projectors are still emerging. All these devices compete for mobility power resources. (Source: Applied Materials)

Insulated gate bipolar transistors (IGBTs), the higher power switching chips used in industrial electronics, electric vehicles (EVs) and electric utilities, are also undergoing manufacturing developments. IGBTs can gain switching performance by thinning the wafer, and market leader Infineon is moving to thinner 300mm wafers for its high-volume bipolar products. Lineback said “using vertical trench structures and wafer thinning improves the switching speed of the IGBTs. But the problem has been that thinning the wafers creates some other problems, and Infineon is always working on improving its trench stop technology.”

EPITAXIAL GROWTH AND DEEP RIE

In all types of power devices, current flows from top to bottom through epitaxial doped regions. For the increasingly popular SJ devices, the

thickness of the doped regions impacts the ON resistance (R_{on}), which controls the switching speed, but making them too thin affects the necessary R_{off} . Bringing the heavily doped columns closer together can improve the performance of power ICs.

Applied Materials has efforts underway to improve the epitaxial, deep reactive ion etching (DRIE), and dense aluminum interconnect deposition steps. For SJ MOSFETs created with the deep trench method instead of the multi-step epitaxial deposition and doping approach, DRIE is the critical difference.

Deep trench SJ MOSFETs have certain advantages. The conventional, and still-mainstream approach, which builds up the epitaxial layers one by one, is relatively time-consuming, requiring multiple thick-epi growth steps followed by dopant implantation and annealing to activate the dopants.

Accurately placing the dopants is challenging.

The deep trench approach, by contrast, involves etching a trench and then backfilling it with highly doped epi films. DRIE, however, requires excellent sidewall profile control, at a high etch rate, with uniformity across the wafer. Deep trench MEMS, such as gyroscopes, can require etching of trenches as deep as 40–50 microns with high precision. Figure 3 shows an example of DRIE for MEMS using Applied’s 200mm etch tool. Deep trench SJ MOSFETs can involve, for example, 60-micron trenches with slightly tapered sidewalls so the trench can be filled without voids (see figure 4).

Mike Rosa, 200mm strategic marketing manager for emerging markets at Applied Global Services, said “for the epi steps, everyone wants high throughput; 40 to 100 microns of epi at greater than 4 microns per

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minute. Once grown, customers need to etch trenches in the blanket film with a DRIE process. The DRIE process must have a high etch rate, as well as the ability to handle slightly tapered structures.”

Subsequent processes include a reduced pressure epi to then fill these structures in a void-free, uniformly doped manner. “With Applied’s DRIE etch tool we can do etch rates of 15 microns per minute, with excellent uniformity across the wafer. That leaves us well positioned to apply it to power chips,” Rosa said.

The critical dimension (CD) of the trench opening is also challenging. Rosa said today’s state of the art is approximately 1 to 2 microns and 40 microns deep. “We can shrink it. Using our DRIE tool, we can shrink the trench CD in a gyroscope to .2 microns or 200 nanometers. The fingers become five times more sensitive as compared to the 1-micron CD structures. With the capabilities of this new etch product, customers can either make the gap smaller and have the same number of fingers, or make the fingers smaller and keep the gap the same, or use fewer fingers,” said Rosa, who earned his doctorate in MEMS technology.

DEEP TRENCH ETCHER

Jon Farr, senior etch product manager, said Applied’s deep trench etch product is targeted primarily at power ICs and MEMS. It features decoupled inductive and capacitive reactor sources. Applied’s DPS source is a two-part chamber, with a lower loading chamber and an upper process chamber. The system offers good uniformity, repeatable performance, low aspect ratio dependence, and long time between cleans (LTBC), Farr said.

“This etch system is aimed at a broad swathe of applications, including power and MEMS. There is interest in making devices with very high aspect ratio (VHAR) submicron trenches from companies making many kinds of

products—optical devices, inkjet heads, even things like blood filters,” Farr said.

SJ power MOSFETs are challenging, partly because the trenches have a high open area due to the pitch, often with a 50% open area and a 10:1 aspect ratio. CDs range from 1 to 5 microns. While the aspect ratio of trenches in memory ICs rarely goes beyond 10:1, deep silicon etch steps are at ratios of 10:1 to 100:1.

Customer applications are divided between single-step etch methods and the Bosch process, each having its specific advantages. The single-step process works well for creating the smooth sidewalls required for miniaturized SJ devices, he said.

While another emerging market, through-silicon vias (TSVs) also requires deep trenches, Farr said TSV trenches are not particularly demanding, and only require low-cost, high-throughput systems. “What we are doing is more difficult. With gyroscopes (MEMS), such a level of precision is required that each device has to be electrically tested. With SJs, there are challenges with the large open area, loading, and CD uniformity.”

Applied’s etcher is a cluster-type tool, capable of plugging in up to four etch chambers. The RF configuration was modernized to improve the across-wafer CD uniformity and provide for higher open areas and improved across-wafer depth uniformity.

“We changed the way the reactor works, with more digital controls requiring more computing power. Customers can configure the system with metal etch, deep trench reactors, strippers, and so on—all on one platform,” Farr said.

Waiting in the wings of the power IC market are two developing processes, one based on gallium nitride (GaN) and one using silicon carbide (SiC), each bearing the challenges associated with compound substrates and the promise associated with wide band-gap materials. With revenues

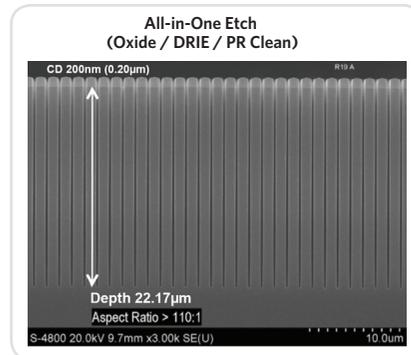


Figure 3. Next-generation devices will require a unique combination of fine CD or sub-micron capability and deep trench etch to produce tightly packed devices with aspect ratios approaching or in excess of 100:1. (Source: Applied Materials)

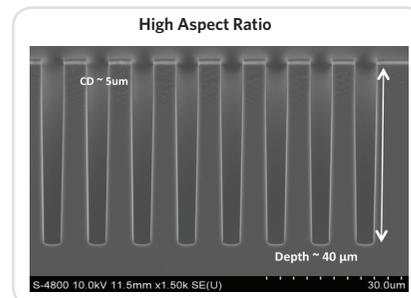


Figure 4. Advanced DRIE solutions for SJ power devices call for exacting control over the sidewall profile, undercut, and selectivity to the oxide and photoresist masks used. (Source: Applied Materials)

growing and multiple companies investing in new manufacturing techniques and materials, the power electronics market will be well worth paying close attention to.

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