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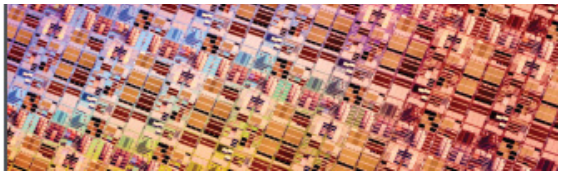

2016 Applied Materials Technical Symposium in Tainan
March 24, 2016
Presentation Abstracts

Exploring New Non-Volatile Memories and Logic beyond 10nm

Time	Title	Presenter
11:00 – 11:15	Welcome	Jackie Tan, Applied Materials
11:15 – 11:50	Future Logic Devices	Prof. Chenming Hu, UC Berkeley
11:50 – 12:50	Lunch	
12:50 – 13:25	Engineering Perpendicular Magnetic Tunnel Junctions for Embedded STT- MRAM through Materials and Process Co-optimization	Chando Park, Qualcomm
13:25 – 13:50	Endura PVD System for Emerging Memory Technology	Kevin Moraes, Applied Materials
13:50 – 14:15	Interconnect Solutions for 10nm and Beyond	Kavita Shah, Applied Materials
14:15 – 14:30	Break	
14:30 – 15:05	Gate-All-Around(GAA): Challenges and Opportunities	Hans Mertens, IMEC
15:05 – 15:30	Implant Solutions for Contact Resistivity Reduction for CMOS 10nm node and Beyond	Vivek Rao, Applied Materials
15:30 – 15:55	Field-effect Transistor Technology Solutions for 10nm And Beyond	Nam Sung Kim, Applied Materials
15:55 – 16:20	Challenges and Opportunities In The Era of More-than-Moore (MTM)	Mike Rosa, Applied Materials
16:20 – 16:25	Conclusion	Jackie Tan, Applied Materials

To register for this symposium, please visit:

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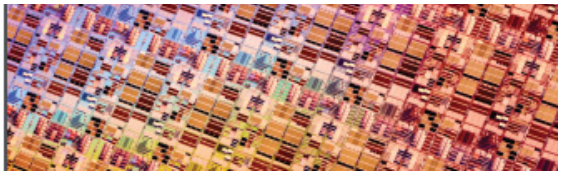

Future Logic Devices

Chenming Hu
Professor, Department of Electrical Engineering and Computer Sciences
University of California Berkeley

FinFET is here. The "thin body" concept that FinFET introduced is a powerful solution for gate length reduction. Solutions for reducing voltage (power) and costs are needed but remain elusive. Nevertheless, some progress has been made.

About the presenter:

Chenming Hu is a Distinguished Professor of Microelectronics at UC-Berkeley. He was formerly the Chief Technology Officer of TSMC and is a board director of Sandisk, Inc. He is known for such innovations as BSIM—the first standard transistor model—and FinFET--the 3D transistor. He has been awarded the IEEE Nishizawa Medal and Andrew Grove Award, the EDAC Phil Kaufman Award, and the UC Berkeley Distinguished Teaching Award. He is a member of the US National Academy of Engineering, the Chinese Academy of Sciences and Academia Sinica. President Obama will present to him the National Medal of Technology and Innovation later this year. He earned his Ph.D. in electrical engineering and computer science from the University of California, Berkeley.

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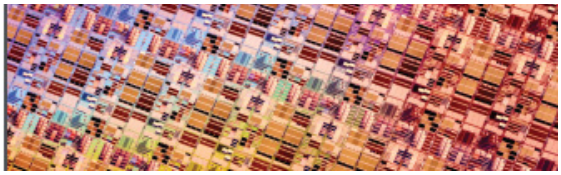

Engineering Perpendicular Magnetic Tunnel Junctions for Embedded STT-MRAM through Materials and Process Co-optimization

Chando Park
Senior Staff Manager
Corporate R&D, ASIC Engineering
Qualcomm Technologies, Inc.

Perpendicular STT-MRAM is considered a leading candidate for an embedded non-volatile memory (NVM) at the 28nm node and beyond due to its high performance, practically unlimited endurance, inherent non-volatility, and logic compatibility. To develop high-performance, high-density STT-MRAM, it is important to systematically link the attributes of materials parameters, process modules, and device characteristics using a dense array of perpendicular magnetic tunnel junctions (pMTJ). This presentation addresses the optimization of all critical pMTJ device parameters in 1 Gbit arrays. Through systematic materials and process co-optimization, all performance requirements were concurrently satisfied, demonstrating that pMTJ-based STT-MRAM is a robust and competitive embedded NVM solution.

About the presenter:

Chando Park is responsible for materials, process and device characterization for STT-MRAM. Before joining Qualcomm in 2013, he worked at HGST and Western Digital, developing advanced read sensors that were successfully transferred to high-volume hard disk drive products. He received his Ph.D. in materials science and engineering from Carnegie Mellon University, has authored more than 20 technical publications, and holds 8 granted patents, with 18 pending.

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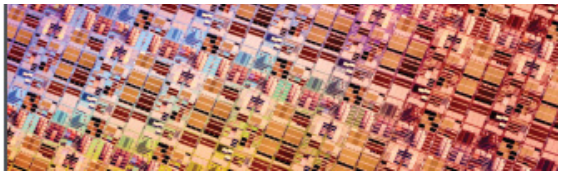

Endura® PVD System for Emerging Memory Technology

Kevin Moraes
Managing Director, Global Product Management
Metal Deposition Products
Applied Materials, Inc.

The opportunity to improve overall CPU performance by addressing the large speed and endurance gaps between DRAM and NAND, as well as the large cost difference between these memories, is creating opportunity for commercializing new Emerging Memory Technologies. Leading candidates are STT-MRAM, Phase Change Memories, and various Resistive Memories. High-volume manufacturing (HVM) of memory cells requires advanced PVD techniques and other integrated processes to create the precise material composition, texture, and interfaces. This presentation focuses on the Endura PVD tool for depositing MTJ stacks with low RA (<10), high TMR (>200%), and few defects. Magnetics and post-patterning data are presented for stacks with an RF MgO barrier; such stacks deliver high performance (TMR/RA and Vbd >1.5V) without adversely affecting defectivity and throughput for HVM. Endura platform options for HVM are included. Dielectric PVD technology used in fabricating Phase Change and Resistive RAM memories will also be addressed.

About the presenter:

Kevin Moraes is responsible for extending Applied's leadership in metals and PVD deposition, and broadening product roadmaps for ALD/CVD and PVD in metal deposition applications. Under his direction, the MDP group has strengthened its lead in its core semiconductor product segments, while developing products for new applications that have significantly grown the business. He earned his Ph.D. in materials science and engineering from Rensselaer Polytechnic Institute, has published 15 papers, and holds 3 patents. He also holds an MBA from the University of California, Berkeley.

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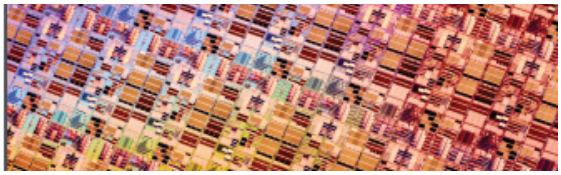

Interconnect Solutions for 10nm and Beyond

Kavita Shah
Interconnect Technology Manager
Transistor and Interconnect Group
Applied Materials, Inc.

Continued interconnect scaling presents unique challenges and exciting opportunities for roadmap advances. Interconnect integration complexity has increased as the industry seeks to optimize yield and cost. At 10nm, the technology objective is to enhance performance while maintaining reliability with copper back-end metallization and low-κ dielectric integration. This presentation reviews innovations for 10nm in deposition technologies and materials that address current challenges and their extendibility to the next node. Promising new materials and technologies appear on the technology roadmap beyond 7nm. The presentation will also examine the relative merits of these new technologies and approaches for integrating the new materials in the overall process flow.

About the presenter:

Kavita Shah helps define the Applied's strategy for next-generation on-chip wiring technology. Previously, as global product manager, she managed a diverse portfolio of PVD, CVD, and ALD products for copper interconnect metallization. In earlier positions as an ALD process engineer and customer applications technologist, she worked on barrier and liner materials and strategic technical engagements with logic and memory customers, respectively. In more than 14 years with Applied, she has successfully enabled key business successes, such as selective CVD metal capping, and contributed strategies to expand product application space. She holds a M. Eng. in chemical engineering from Cornell University.

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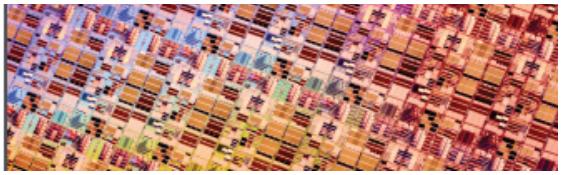

Gate-All-Around (GAA): Challenges and Opportunities

Hans Mertens
Senior Researcher
imec

Gate-all-around (GAA) nanowire transistors are promising candidates to replace FinFETs at sub-10nm CMOS nodes. They offer optimal electrostatic control, thereby enabling ultimate CMOS device scaling. In a horizontal configuration, nanowire transistors are a natural extension of today's mainstream FinFET technology. In this talk, GAA devices will be introduced. After that, challenges and opportunities will be highlighted from the process integration perspective.

About the presenter:

Hans Mertens currently researches horizontal gate-all-around process integration based on group-IV semiconductors. Before joining imec in 2012, he was on the staff of NXP Semiconductors, where he worked on SiGe BiCMOS technologies for RF small-signal applications. He earned his Ph.D. in physics from Utrecht University in The Netherlands. Publications, patents?

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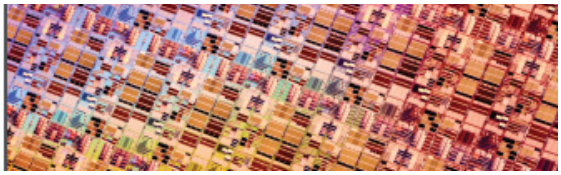

Implant Solutions for Contact Resistivity Reduction for CMOS 10nm node and Beyond

Vivek Rao
Member Technical Staff
Field Applications/VSE
Applied Materials, Inc.

The reduction in contact CD with CMOS scaling adversely increases silicide contact resistance, which has become a dominant component of R_{SD}, thus affecting CMOS transistor performance. The 10-7 nm nodes require that the specific contact resistivity be reduced to < 1E-9 $\Omega.cm^2$. This presentation addresses the integration of implant solutions in the contact module for advanced CMOS logic, DRAM, and Flash memory, and summarizes the results of contact resistivity reduction achieved at Applied Materials.

About the presenter:

Vivek Rao focuses on strategic marketing and ion implant applications for a wide range of global customers, and is a key member of the contact module process development team. He previously gained extensive experience in CMOS, BiCMOS, DRAM, and flash technology and product development with IBM, Texas Instruments, Infineon, and Motorola. He earned his Ph.D. in materials science from The University of Arizona and an MBA from Babson College, has published 25 papers, and holds 18 patents.

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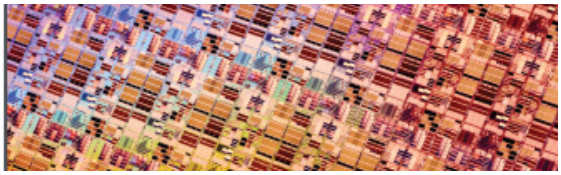

Field-effect Transistor Technology Solutions for Sub-7nnm

Namsung Kim
Director in Advanced Product Technology Development
Applied Materials, Inc.

After successful transition from planar to FinFET technology at the 22nm node, the 16/14nm node is now in mass production; enabling continued CMOS scaling (Moore's law) primarily through FinFET-enhanced electrostatic control. However, looking ahead to the 10nm/7nm nodes and beyond, major challenges and roadblock remain, including further FinFET scalability issues. This presentation explores ultimate CMOS transistor technology scaling challenges and their potential solutions in light of new materials and processing techniques, including transistor evolution from FinFET to horizontal gate-all-around. Challenges addressed include advanced channel materials, gate stacks, parasitic capacitance, and contact resistance shared by all of the architectures.

About the presenter:

Namsung Kim leads the Transistor Technology Team working on transistor scaling and related future inflections. He has more than 20 years' experience in FEOL integration and devices from foundry (GLOBALFOUNDRIES and SSMC) and memory manufacturers (SK-Hynix). His extensive engineering and management experience spans transistor development and volume production from poly/SiON to high-k metal gate low-power and high-performance technologies across planar and FinFET technologies. He earned his M.S. in electrical and computer engineering from the National University, Singapore, has authored several dozen technical publications, and holds 30 patents.

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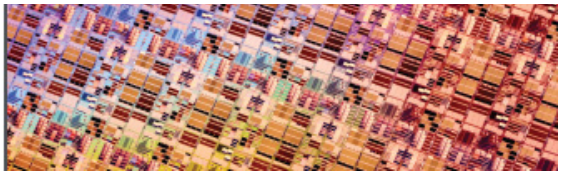

Challenges and Opportunities In The Era of More-than-Moore (MTM)

Mike Rosa
Director of Product Strategy & Technical Marketing
200mm Equipment Product Group
Applied Materials, Inc.

Once termed 'emerging technologies,' the More-Than-Moore (MTM) device technologies, as they are now more widely known, include MEMS, power devices, CMOS image sensors, and various packaging schemes. With the proliferation of the smart phone and the ongoing evolution of Advanced Driver Awareness and Safety (ADAS) capabilities showcased in the automotive market, MTM device technologies now promise to become far more ubiquitous in our increasingly gadget-filled lives. What does this mean for the 200mm/300mm traditional semiconductor market? What challenges and opportunities do MTM market trends and the technology requirements present to the fab/foundry and semiconductor equipment vendor? This presentation will explore these questions and present a number of new material and process technologies that are enabling MTM device manufacturers to chart a course toward the next generation of MTM devices.

About the presenter:

Mike Rosa identifies key device technology inflections to develop roadmaps for equipment and processes to support More-than-Moore device technologies. With more than 18 years in the industry, he has gained significant MEMS domain knowledge and technology commercialization expertise, having developed MEMS-based solutions for xerography and ink-jet printing, photonics, optical switching, and laser/VCSEL integration and packaging. Previously, he worked at Xerox Corp., PARC Inc., Australian Microelectronics Centre, and National ICT Australia. He holds a Ph.D. in MEMS Design/Fabrication and an MBA, has authored over 40 technical publications, and holds over 25 U.S. patents.