Transmission Line Protection – End to End Testing

Hands on Relay School, March 15, 2018

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Presentation Agenda

• Why do you need Communications Aided/Based Tripping Schemes?

• How do you build one? Design.

• Are you sure it works? Testing.

• What can go wrong? Troubleshooting.

• The fun part. Lab Testing.
Why do you need Communication Aided Tripping?
Why do you need Communication Aided Tripping?

- Traditional step distance or time overcurrent protection is not adequate due to:
  - System Stability
  - Thermal Damage
  - Protection Limitations
Line Protection without Communication

- Step Distance using impedance (21), definite time delayed (67) overcurrent, and time overcurrent (51) elements.

- Delayed Clearing at remote end of the line in either direction
Line Protection without Communication
How to build a Communication Aided/Based Protection Scheme?
100% High speed clearing - Option 1

- Utilize existing (single end) protection elements
  - Impedance/Distance, Phase and/or Ground
  - Definite and Time Overcurrent, Phase and/or Ground
  - Traveling Wave / Rate of change (dV/dt, dI/dt)

- Assign specific elements to bit(s)/tone(s) and transmit to the remote terminal

- Use local protection elements, bits/tones received from the remote end(s), and logic to either trip or restrain trip with little to no intended time delay.
Directional Under-reaching Transfer Trip (DUTT)

- Uses instantaneous elements (e.g. Zone 1, inst 50/67) to send a bit/tone to trip remote terminal(s) of the line.
Directional Under-reaching Transfer Trip (DUTT)
Directional Under-reaching Transfer Trip (DUTT)
Permissive Over-reaching Transfer Trip (POTT)

- Uses overreaching elements (e.g. Zone 2, 67G2) to send a bit/tone giving permission to the remote terminal(s) of the line that it may trip if it too sees a fault.

- If all terminals agree there is a fault in the forward direction it must be on the line.
Permissive Over-reaching Transfer Trip (POTT)

- Simplified POTT Scheme
Permissive Over-reaching Transfer Trip (POTT)

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Permissive Over-reaching Transfer Trip (POTT)

- Scheme is enhanced with a reversed element (Zone 3, 67G3) to block the POTT scheme and prevent false tripping during a current reversal.
Permissive Over-reaching Transfer Trip (POTT)

- Additional enhancements:
  - Weak end infeed
  - Echo back
  - ‘b’ repeat
Directional Comparison Blocking (DCB)

- Uses a local overreaching element (e.g. Zone 2) to trip and a remote reversed element (e.g. Zone 3) to block the tripping element.

- Local overreaching element is briefly delayed (1 - 5 cycles) for communication latency, i.e. waits for a block signal.
Directional Comparison Blocking (DCB)

Substation A

Zone 2
Def Time Overcurrent

PU

DO

Trip Breaker

Zone 3 (Reverse)

Block

Substation B

Zone 2
Def Time Overcurrent

PU

DO

Trip Breaker

Block

Zone 3 (Reverse)
Directional Comparison Blocking (DCB)

- Zone 2 – DCB Only
- Zone 3 – DCB Block
- Zone 2 Local AND NOT Zone 3 Remote

Substation A

Substation B
Directional Comparison Blocking (DCB)

- 67G2 Local AND NOT 67G3 Remote
- 67G3 – DCB Block
- 67G2 – DCB Only
- 67G2 Local AND NOT 67G3 Remote
Additional Schemes

• Drive to lockout
  – Used to signal to the remote end not to attempt a reclose
  – Avoids reclosing into damaged equipment from the remote terminal
  – Typically used for breaker failure, transformer terminated lines, or series capacitors
100% High speed clearing - Option 2

- Build a current differential!

- Current in = Current out. Sounds easy!

- Communicate AC quantities to the remote terminal in near real-time and calculate the difference.

- The devil is in the details.
Line Current Differential

• Encodes the locally measured AC signal and transmits it to the remote terminal(s).

• Each relay must time align local and remote measurements to calculate an operate quantity.
  – Ping Pong vs Timestamping

• Prevent false tripping for CT saturation and Open CT
Line Current Differential

• Disable differential when comm channel is bad or unstable.

• Long Lines – charging current

• No PTs required

• Zone of protection is clearly defined
Line Current Differential

- Substation A
- Substation B

Line Differential
Communication Systems

- Different schemes require certain levels of communication service:
  - Could the communication channel be effected during a fault?
  - Does the scheme require comm during a fault to work?
  - What is the channel latency?
  - Is channel latency consistent? Deterministic.
  - Is the channel latency the same in both directions? Asymmetry.
The Buddy System of Line Protection
Are you sure it works?
Testing

• End to end testing is designed to test logic missed by element testing and single end testing

• Verifies:
  – Communication channel and addressing
  – Comm Aided/Based Protection Logic
  – Engineers protection settings
  – Breaker trip and close circuits (if tripping to breaker)
End to End Testing

• Schemes are tested by playing faults into all relays associated with a scheme.

• Faults must be precisely time aligned to work properly
  – Remember 8ms is almost a 180 degree phase shift at 60 Hz

• Simulated faults are usually built by the protection engineer to check specific points where misoperation could occur.
Misoperation – NERC Definition

1. Failure to Trip – During Fault
2. Failure to Trip – Other Than Fault
3. Slow Trip – During Fault
4. Slow Trip – Other Than Fault
5. Unnecessary Trip – During Fault
6. Unnecessary Trip – Other Than Fault
NOT a Misoperation

“A Composite Protection System operation that is caused by personnel during on-site maintenance, testing, inspection, construction, or commissioning activities is not a Misoperation.”

Typical Line

Communication Medium: PLC, Direct Fiber, Copper, SONET, Packet Switched, etc
Typical Test Configuration

Substation A

Relay A

GPS

Test Set A

Breaker Sim

Va, Vb, Vc

Ia, Ib, Ic

Communication Medium:
PLC, Direct Fiber, Copper,
SONET, Packet Switched, etc

Substation B

Relay B

GPS

Test Set B

Breaker Sim

Va, Vb, Vc

Ia, Ib, Ic

High Accuracy Clock Signal
Faults to Run

• Both Phase (3LG, LL) and Ground (SLG, 2LG)
• Possibly different phases of the same fault if single pole tripping
  – Phase segregated direct trip or permissive trips
• Fault at points where scheme is need for high speed clearing
  – Mid line, high impedance fault.
  – Line end
Faults to Run

- No-op Faults
  - Parallel Line fault and clear (current reversal)
  - Slow clearing faults on lines “behind” relay
  - Tapped loads
- Pay attention to 3 phase PT location
- Reclosing requirements
- Pre-fault
### Results – Sequence of Events

<table>
<thead>
<tr>
<th>#</th>
<th>DATE</th>
<th>TIME</th>
<th>ELEMENT</th>
<th>STATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>244</td>
<td>03/14/2018</td>
<td>22:28:56.434</td>
<td>TRGTR</td>
<td>Asserted</td>
</tr>
<tr>
<td>243</td>
<td>03/14/2018</td>
<td>22:28:56.443</td>
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<tr>
<td>242</td>
<td>03/14/2018</td>
<td>22:29:50.491</td>
<td>51G</td>
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<tr>
<td>241</td>
<td>03/14/2018</td>
<td>22:29:50.491</td>
<td>67G4</td>
<td>Asserted</td>
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<tr>
<td>240</td>
<td>03/14/2018</td>
<td>22:29:50.499</td>
<td>Z2G</td>
<td>Asserted</td>
</tr>
<tr>
<td>239</td>
<td>03/14/2018</td>
<td>22:29:50.499</td>
<td>Z4G</td>
<td>Asserted</td>
</tr>
<tr>
<td>238</td>
<td>03/14/2018</td>
<td>22:29:50.499</td>
<td>KEY</td>
<td>Asserted</td>
</tr>
<tr>
<td>237</td>
<td>03/14/2018</td>
<td>22:29:50.499</td>
<td>TMB1A</td>
<td>Asserted</td>
</tr>
<tr>
<td>236</td>
<td>03/14/2018</td>
<td>22:29:50.574</td>
<td>Z2G</td>
<td>Deasserted</td>
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<tr>
<td>235</td>
<td>03/14/2018</td>
<td>22:29:50.574</td>
<td>Z4G</td>
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<tr>
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<td>03/14/2018</td>
<td>22:29:50.574</td>
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<tr>
<td>233</td>
<td>03/14/2018</td>
<td>22:29:50.574</td>
<td>TMB1A</td>
<td>Deasserted</td>
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<td>Deasserted</td>
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<td>22:35:50.487</td>
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<tr>
<td>229</td>
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<td>22:35:50.492</td>
<td>67G4</td>
<td>Asserted</td>
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<tr>
<td>228</td>
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<td>22:35:50.496</td>
<td>Z2G</td>
<td>Asserted</td>
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<tr>
<td>227</td>
<td>03/14/2018</td>
<td>22:35:50.496</td>
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<td>22:35:50.496</td>
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<tr>
<td>225</td>
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<td>TMB1A</td>
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<td>SV1</td>
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<tr>
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<tr>
<td>222</td>
<td>03/14/2018</td>
<td>22:35:50.829</td>
<td>OUT101</td>
<td>Asserted</td>
</tr>
</tbody>
</table>
Results – Oscillography
What can go wrong?
DC Circuits and Logic

• Bad Breaker Status
  – Switch on to fault

• Bits/Tones not the same on both ends
  – Differing utility standards

• Relay is not fully isolated
  – False trip

• Relay is too isolated
  – Reclosing enable/disable or Hot Line Hold switch
AC Circuits

• Incorrect wiring between:
  – Relay and test switches
  – Test switches and test set

• Test Set Limitation
  – Engineer needs to redefine faults
  – High current test set

• Different phasing between utilities
Communications

• Comm Circuits
  – Transmit / Receive Rolled
  – Circuit is looped back in comm equipment
  – Circuit was never commissioned

• Wrong equipment
  – Multimode vs Single mode fiber
  – Fiber optic transceivers

• Addressing

• Bad circuit – Bit error, noise, corrupting data
Questions??
LAB – Initial Wiring

• Power (AC plug)
• AC Input into Relay from Test Set
  – 3 Phase Voltage
  – 3 Phase Current
• Relay DC Inputs
  – Breaker Status
• Relay AC Outputs
  – Trip and Close
• Communications
  – Fiber - Differential Channel
  – Copper RS232 – POTT / DUTT bit channel
LAB – Initial Wiring

• Verify testing setup
  – Is the relay seeing ABC rotation of voltage and current?
  – Can the relay trip/close the “breaker”?
  – Are the relays communicating?
    • Differential
    • POTT / DUTT
Protection Design – Phase Elements

• 4 Mho Phase Distance
  – Zone 1 – Instantaneous trip (80% of line)
  – Zone 2 – POTT Keying Only (200% of line)
  – Zone 3 – POTT Reverse Blocking (200% of line)
  – Zone 4 – Traditional Zone 2 (120% of line)
    • 20 cycle delay
B-A 21P  Type=SEL311P
SUB B 230 kV
CTR=240 PTR=2000
Zone 1: Z1P=5.24  Z1PD=0cy
Zone 2: Z2P=13.11  Z2PD=0cy
Zone 3: Z3P=13.11  Z3PD=0cy
Zone 4: Z4P=8.53  Z4PD=20cy
Line Z= 6.55@ 84.1 sec Ohm (54.61 Ohm)

A-B 21P  Type=SEL311P
SUB A 230 kV
CTR=240 PTR=2000
Zone 1: Z1P=5.24  Z1PD=0cy
Zone 2: Z2P=13.11  Z2PD=0cy
Zone 3: Z3P=13.11  Z3PD=0cy
Zone 4: Z4P=8.53  Z4PD=20cy
Line Z= 6.55@ 84.1 sec Ohm (54.61 Ohm)
Protection Design – Ground Elements

• 4 Quadrilateral Ground Distance
  – Zone 1 – Instantaneous trip (80% of line)
  – Zone 2 – POTT Keying Only (200% of line)
  – Zone 3 – POTT Reverse Blocking (200% of line)
  – Zone 4 – Traditional Zone 2 (120% of line)
    • 20 cycle delay
Protection Design – Ground Elements con’t

• 3 Definite Time Ground Overcurrent
  – 67G1 – Instantaneous trip (~80% of line)
  – 67G2 – POTT Keying Only
  – 67G3 – POTT Reverse Blocking